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A study on the material and device characteristics of hafnium oxynitride MOSFETs with TaN gate electrodes

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by

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Dedication

This works are dedicated to my lovely wife, kids; and family across the Pacific Ocean.

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A study on the material and device characteristics of hafnium oxynitride MOSFETs with TaN gate electrodes

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HfO_2 have been under intense investigation for gate dielectric application into the 70 nm technology nodes and beyond to replace conventional SiO_2 or oxynitrides since it possesses a dielectric constant of 22 – 25, a large band gap of 5.6 eV with sufficient band offsets of larger than 1.5 eV, and is thermally stable in contact with silicon and metal gates. However, HfO_2 is vulnerable to the diffusion of oxygen that causes formation of a low-k interfacial (silicon oxide or silicate) layer at the Si interface and boron penetration when combined with the p^+ poly-Si gate technology. In addition, HfO_2 crystallizes at relatively low temperature (<600 ºC) unlike SiO_2 that remains in amorphous phase through the semiconductor process involving high temperature annealing higher than 1000 ºC.

In this research, the focus was placed on the effects of nitrogen in HfO_2 dielectrics to improve thermal stability (i.e. equivalent oxide thickness (EOT)

increase by anneal and crystallization) of the dielectrics by surface treatment and nitrogen incorporation into the HfO_2. In addition to the Hf-based dielectrics themselves, effects of Hf into conventional SiO_2 dielectrics and the characteristics of TaN for gate electrode application were studied.

The effects of Hf implanted into p-type Si substrates on the properties of n^+ polycrystalline-Si/SiO_2/Si capacitors and MOSFETs have been investigated. Flat-band voltages (V_{fb}) and substrate doping concentrations (N_A) calculated from high frequency C-V curves of the capacitors were not dependent on the doses of Hf. Also, electron channel mobility was not degraded by Hf contamination. The amount of Hf diffused into the Si substrate during the high-k dielectric imposed negligible effects on silicon based MOS device characteristics in terms of C-V, J-V characteristics and electron mobility.

In this work, sputtered-TaN was mainly used as a gate electrode. Work functions of tantalum nitride (TaN) film before and after post-metal-annealing were ~ 4.15eV, and ~ 4.7 eV, respectively.

A surface nitridation technique using NH_3 anneal has been investigated to reduce interfacial reactions and consequently the equivalent oxide thickness (EOT) of TaN/HfO_2/ Si MOS capacitors. For the same EOT, the nitrided samples showed 1 ~ 2 order of magnitude lower leakage current density compared to the non-nitrided ones. However, nitridation induced higher interface state density and larger hysteresis. The degraded interface quality due to the nitridation was improved by post-metal annealing (PMA).

Electrical and material characteristics of hafnium oxynitride (HfON) gate dielectrics have been studied in comparison with HfO_2. HfON was prepared by a deposition of HfN followed by post-deposition-anneal (PDA). By secondary ion mass spectroscopy (SIMS), incorporated nitrogen in the HfON was found to pile up at the dielectric/Si interface layer. Based on the SIMS profile, the interfacial layer (IL) composition of the HfON films appeared to be similar to hafnium-silicon-oxynitride (HfSiON) while the IL of the HfO_2 films seemed to be hafnium-silicate (HfSiO). HfON with nitrogen of ~ 5 atomic % at the interface resulted in an increase in crystallization temperature, higher dielectric constant, lower leakage current at the same equivalent oxide thickness (EOT) and high dielectric strength compared to HfO_2. The improved electrical properties of HfON over HfO_2 can be explained by the thicker physical thickness of HfON for the same EOT due to its higher dielectric constant as well as a more stable interface layer. High temperature forming gas anneal at 600^{o}C for 30 min was effective in improving carrier mobility of nMOSFETs with HfON gate dielectrics.

The effects of silicon and nitrogen profiles in gate dielectrics on the electrical and material properties of the Hf-based dielectric were investigated. To vary nitrogen profiles in the HfON films, 6-Å-thin Si layers were inserted in the different position of HfON films. By the insertion of Si layer, nitrogen profiles were modulated. The inserted Si leading to the nitrogen incorporation increased thermal stability. Highest mobility was observed at the dielectrics with Si layer inserted in the middle of HfON films.

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Chapter 1: Introduction and Motivation

1.1 WHY HIGH-K GATE DIELECTRICS?

Since 1960, which saw the inception of the metal-oxide-semiconductor field effect transistor (MOSFET), the most important device for modern integrated circuits, thermally grown silicon oxide (SiO_2) has been used as gate dielectrics because of its advantages: 1) the electrically stable Si-SiO_2 interface (i.e. $D_{it} \sim 2x10^{10}$ $eV^{-1}cm^{-2}$), 2) the high dielectric breakdown strength (≥ 10 MV/cm) and 3) the thermal stability at high temperature (remaining in amorphous state after the integration processes) [1]. For the last four decades, the improvement of speed and shrinkage of chip area of integrated circuits were achieved by scaling down of physical thickness of the SiO_2 gate dielectrics and gate length (L).

However, beyond the 100 nm node technology, SiO_2 has reached its physical limitations: higher leakage current and reliability concerns. As shown in Table 1.1, continuing scaling down of the MOSFET device with the minimum feature size of 90 nm and below requires EOT (Equivalent Oxide Thickness) less than 15 Å. A 10-15Å-thick SiO_2 layer corresponds to only around 3-4 mono-layers of SiO_2. In this thinner EOT range, SiO_2 suffers from leakage current too high to be used (particularly) for low power operation due to the direct tunneling of electrons as shown Fig. 1.1 [3].

		2003	2005	2007	2009	2012	2015	2018
Gate Length (nm)		107	80	65	50	30	25	18
EOT (nm)	**High Speed**	1.3	1.2	0.9	0.8	0.7	0.6	0.5
	Low Power	1.6	1.4	1.2	1.0	0.9	0.8	0.7
S/D Junction Depth (X_j, nm)*		49.5	35.2	27.5	NA	NA	NA	NA
Interconnect Levels		9	11	11	12	12	13	14
Logic V_{DD} (V)	**High Speed**	1.2	1.1	1.1	1.0	0.9	0.8	0.7
	Low Power	1.0	0.9	0.8	0.8	0.7	0.6	0.5

** Beyond 2007, X_j has no significance since Xj is assumed to be with the drain extension in ITRS taxonomy.*

Table 1.1 Minimum feature size (in printed gate length) and EOT for high-speed devices (i.e. MPU) and low power devices from 2003 ITRS roadmap [2].

In addition, SiO_2 thickness uniformity across a 12 inch wafer imposes even more crucial difficulty in the growth of such a thin film, since even a mono-layer difference in thickness represents a large percentage difference and thus can result in the variation of threshold voltage (V_t) across the wafer [4]. Reliability also becomes a huge concern for a SiO_2 film only 10-15Å thick [5, 6].

Dielectrics with higher dielectric constant than that of SiO_2 or high-k dielectrics have been under intense investigation in order to replace SiO_2. High-k dielectrics provide the same capacitance with a thicker film thickness (t) as the capacitance achieved using physically thinner SiO_2 by equation (1) where C represents capacitance, k is dielectric constant, ε_o is the permittivity of free space - a constant, A is capacitor area, and t is dielectric thickness.

$$C = k\varepsilon_o \frac{A}{t} \qquad (1.1).$$

Leakage current of SiO_2 is governed by Fouler-Nordheim tunneling where conduction occurs by field assisted electron tunneling at the field range of $V_i \equiv E_i d > \phi_B$ while direct tunneling of electrons at the lower field $V_i \equiv E_i d < \phi_B$ where V_i, E_i, and ϕ_B represent voltage applied to dielectric, electric field across dielectric and barriers height between gate electrode and dielectric, respectively [7]. In other words, as the thickness of SiO_2 becomes thinner, leakage current is more likely to be governed by direct tunneling current which increases significantly as thickness becomes thinner by equation (1.2).

$$J = \frac{A}{d^2} \cdot \left\{ \left(\Phi_B - \frac{V}{2} \right) \cdot \exp\left(-B \cdot d \cdot \sqrt{\Phi_B - \frac{V}{2}} \right) - \left(\Phi_B + \frac{V}{2} \right) \cdot \exp\left(-B \cdot d \cdot \sqrt{\Phi_B + \frac{V}{2}} \right) \right\} \qquad (1.2),$$

where $A = \frac{q^2}{2\pi h}$, $B = \frac{4\pi\sqrt{2m^* q}}{h}$, and ϕ_B is barrier height, respectively. In equation (1.2), q, m^*, and h represent electron charge, effective mass of electron, and Plank's constant, respectively.

Therefore, by using physically thicker high-k dielectrics for the same EOT, leakage current can be reduced by several orders as shown in Fig. 1.1. In the next subsection, high-k dielectrics as candidates for MOSFET application will be briefly reviewed.

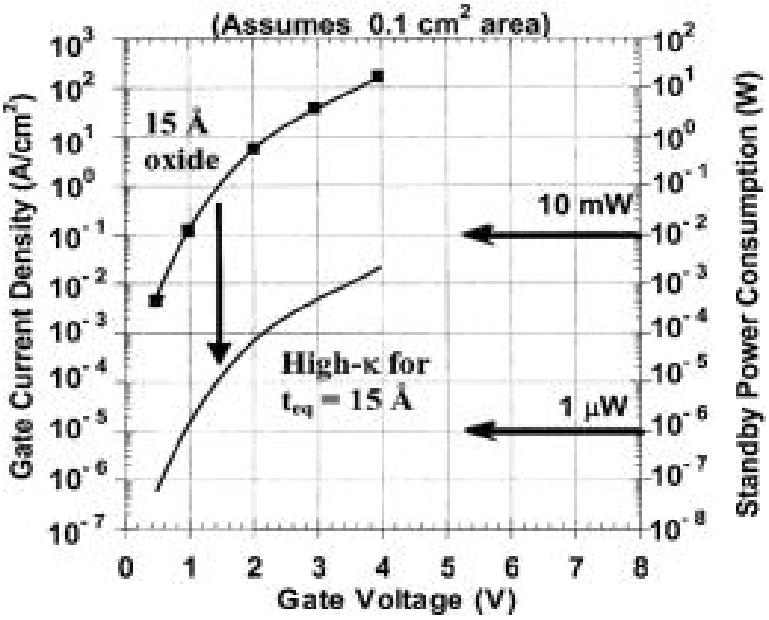


Figure1.1 Comparison of leakage current density of SiO_2 (EOT=15 Å) over high-k dielectric with the same EOT [3].

1.2 HfO_2 AS A HIGH-K GATE DIELECTRIC

High-*k* gate dielectrics have been studied as alternative gate dielectrics for the 70 nm technology node and beyond to replace conventional SiO_2 or silicon oxynitrides (SiO_xN_y). Principal requirements for high-k dielectric applications are 1) high dielectric constant 2) high band offset with electrodes (i.e. barrier height) to suppress leakage current 3) thermally and chemically stable in contact with Si substrate. In Fig. 1.2, dielectric constants of high-k candidates were summarized. TiO_2 and barium strontium titanate (BST) showing profoundly higher k in Fig. 1.2, were reported not to be thermally stable with silicon substrates [8]. It is worth mentioning that high-k dielectrics such as BST with a too high dielectric constant (>100) does not seem to be appropriate since the high dielectric constant causes field induced barrier lowering (FIBL) which degrade short channel effects of MOSFETs [9].

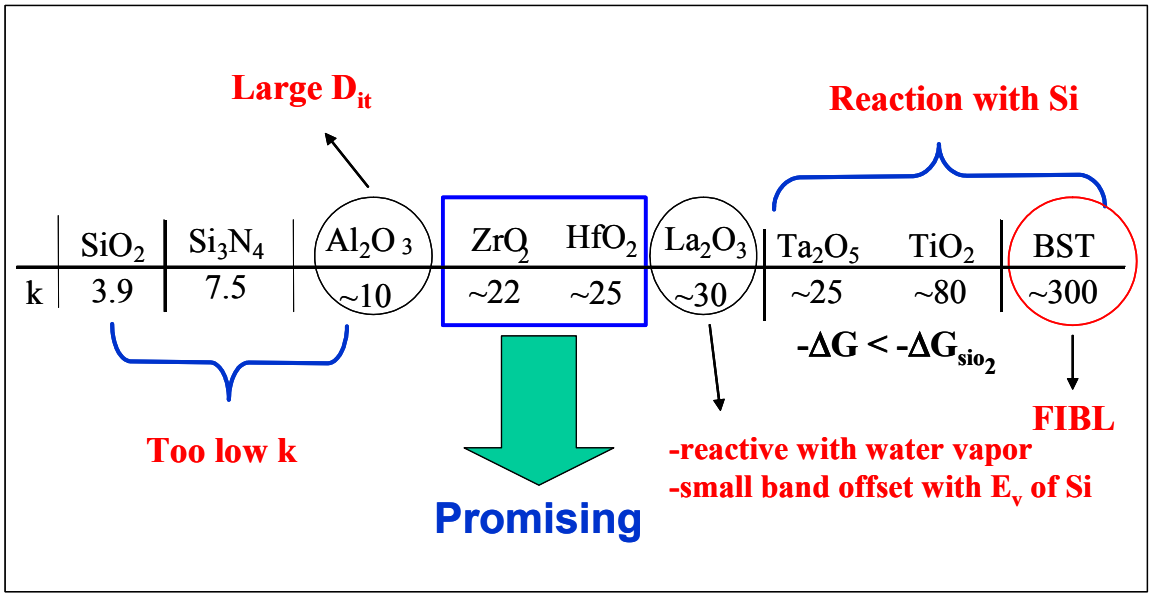


Figure 1.2 Various gate dielectrics and their dielectric constants, and concerns for the application into gate dielectrics [10, 11, 12, 13].

Band offsets of high-k dielectrics with the conduction band edge (ϕ_{Be}) and valence band edge ϕ_{Bh} of Si are compared in Fig. 1.2. The higher band offset indicates that carriers are less likely to be injected from an electrode into a dielectric film. According to a report [3], band offset less than 1.0 eV may lead to an unacceptably large leakage current. Based on the band offset in Fig. 1.2, Ta_2O_5, which has been studied widely for the application in DRAM storage capacitors appears to be inappropriate for the gate electrode application. Al_2O_3 and Si_3N_4 have too low k to be used for several generations as shown in Fig.1.2. Among these materials, HfO_2 has been shown to be compatible with poly-silicon gate [15, 16], poly-SiGe [17], and TaN gates [18]. In contrast, ZrO_2 has been reported that it was not compatible with poly-Si gate due to the reaction of Zr with poly-Si gate [19].

MOSFETs with HfO_2 dielectrics and TaN gate showed very low EOT (~10-12Å) and low leakage current even after the conventional CMOS process flow [18]. Considering the cost of development and implementation, HfO_2 gate dielectric needs to span two or three generations from the 75 nm to the 35 nm design rule. To meet the requirements for these generations, EOT should be scaled down to less than 10 Å while suppressing leakage current to below 1 A/cm^2 [3].

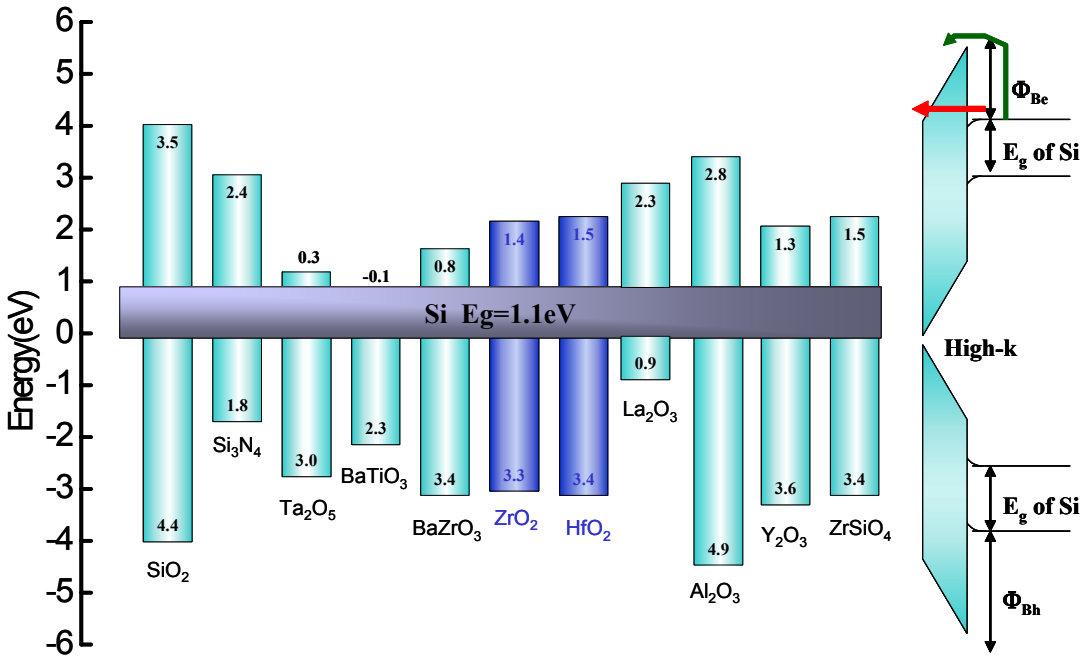


Figure 1.2 Band offset of gate dielectric candidates with conduction band edge and valence band edge of Si substrate [14].

1.3 RATIONALE OF NITROGEN INCORPORATION INTO THE HAFNIUM OXIDE

1.3.1 Nitrogen incorporation in SiO_2 gate dielectrics

Nitrogen incorporation technology has been extensively investigated in the thermal SiO_2 gate dielectrics to suppress impurity penetration [20] and improve reliability [21]. Table 1.3 summarized the major advantages and disadvantages of nitrogen incorporated silicon oxide (SiO_xN_y) formed by using NH_3 gas as a nitrogen source. SiO_xN_y has been used since the mid-80's to replace SiO_2 in the area of flash memory which demands a more reliable dielectric than SiO_2. Even though the rationale of nitrogen incorporation into high-k dielectrics is similar to that of the introduction of SiO_xN_y gate dielectric, more attention should be paid to the additional reasons and differences from SiO_xN_y.

Advantages	Disadvantages
• Suppressed diffusion or boron penetration [20] • High dielectric strength [20] • Enhanced resistance to high-field stress [21] • Radiation hardness [22]	• High-density of fixed charges and interface states [23] • Degraded mobility [24] • High-density electron traps due to large amount of hydrogen [25]

Table 1.3. Advantages and disadvantages of SiO_xN_y gate dielectric over thermal-SiO_2 film.

Single oxide high-k dielectrics such as HfO_2 and ZrO_2 are vulnerable to the diffusion of oxygen which causes formation of a low-k interfacial (silicon oxide or silicate) layer at the Si interface. EOT of HfO_2 with an initial EOT of ~10 Å increase more than ~4Å during the post-metal-deposition anneal (PMA) at ~950 ºC. This EOT increase would limit the use of high-k dielectrics.

Single oxide high-k dielectric remains in crystalline phase after post-metal-annealing (PMA, i.e. annealing after gate electrode formation) unlike SiO_2 which remains in amorphous phase through the semiconductor process. Nitrogen incorporation into metal oxide is expected to retard crystallization of metal oxides [26].

1.3.2 Nitrogen incorporation in the high-k dielectrics

In the field of high-*k* dielectrics, TaO_xN_y formed by Ta_2O_5 deposition and subsequent NH_3 anneal was reported [27]. However, there have been very few reports on HfO_2 gate dielectrics [28]. Recently, several studies have focused on the improvement of the thermal stability of high-k gate dielectric to overcome the dielectrics' insufficient immunity to oxygen or impurity diffusion during the subsequent thermal process. Those studies include an NH_3 nitridation of the Si surface [17], an addition of Al into HfO_2 ($HfAl_xO_y$) [29, 30], an incorporation of nitrogen into ZrO_2 (ZrO_xN_y) [31], and capping a HfO_2 layer with a nitrogen-incorporated layer [28]. However, those processes have additional process steps or involve hydrogen impurity from NH_3. In this work, a novel technique to fabricate HfON, which does not involve any additional process steps or hydrogen impurity, will be presented. In addition, the new method appears to be much more promising since HfON is compatible both with poly-Si and metal gates unlike ZrO_xN_y [32] which is not compatible for poly-Si process.

For the ultra-thin regime (i.e. EOT < 10Å), penetration of oxygen and impurities should be suppressed to maintain low EOT and reduce flat band voltage fluctuation. In particular, boron diffusion into the gate dielectric and substrate is one of the major concerns in poly-Si gate devices [4]. Fig. 1.3 summarizes the advantages and disadvantages in terms of crucial concerns for MOSFET applications of recent studies on the nitrogen incorporation into the HfO_2 films.

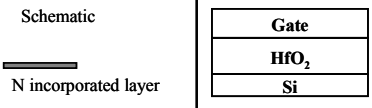
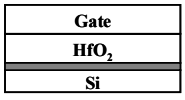
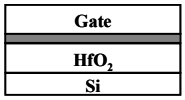
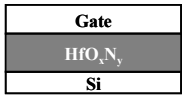
	HfO_2	Bottom Nitridation (BN) [16, 17]	Top Nitridation (T(S)N) [28, 33]	HfO_xN_y [34, 35]
Schematic N incorporated layer				
Interface quality	***	*	****	**
Impurity diffusion	*	***	**	****
EOT control/Scalability	*	***	**	****
Crystallization	*	*	**	****
Process complexity	****	**	*	****

Figure 1.3 Comparison of nitrogen incorporation techniques with HfO_2 in terms of required properties for the gate dielectric applications. The more stars indicates the more advantages.

Nitridation of Si surface (SN) using NH_3 prior to a deposition of high-*k* dielectric has been shown to be effective in achieving low EOT and preventing boron penetration [16, 17]. However, this technique results in higher positive interface charges [27], which lead to higher hysteresis and reduced channel carrier mobility. An additional demerit of SN is the presence of residual hydrogen coming from NH_3 gas which has deleterious affects on the charge trapping behaviors of MOSFET devices [36]. One unique advantage of SN is that it provides a useful tool for the pre-treatment of substrate which can be applied to the various dielectric deposition methods such as chemical vapor

deposition (CVD) or atomic layer deposition (ALD) as well as physical vapor deposition (PVD).

Top nitration (TN) on the HfO_2 is demonstrated by the deposition of HfN on a HfO_2 layer to improve diffusion immunity without degrading interface quality [28]. For the TN process, two annealing processes are involved: one is the post-deposition annealing to form the HfO_2 layer and the second is a post-HfN[1] deposition anneal. Despite the complicated processes, the TN process provides an ideal nitrogen profile which would contribute to understanding the role of interface and impurity diffusion in high-k films. Recently, a structure with HfSiON layer on the top of HfO_2 (TSN) has been reported to be more effective in suppressing impurity penetration and EOT increase during PMA process [33]. The improvement in the TSN over TN has been attributed to the higher nitrogen concentration in the TSN than that of the TN sample.

Fully nitrided (FN) HfO_2 layer (i.e. HfON) is formed by deposition of HfN followed by post-deposition anneal (PDA) with the same process steps as in the HfO_2 films. Except interface quality that is degraded by the presence of nitrogen, FN films are expected to have advantages for other required properties compared to TN, SN, and HfO_2. FN samples show the best thermal stability among the method in Fig.1.3 because nitrogen bonds exist in the bulk-dielectric as well as at the dielectric/Si interface. The details of the thermal stability and chemical bonding structures will be described in the next chapter.

Recently, there have been several reports [37-40] on the incorporation of both Si and N into HfO_2 (i.e. HfSiON, hafnium silicon oxynitride) which was found to improve thermal stability further compared to HfON. Especially, M.R. Visokay et al. performed comparative study on the effects of nitrogen incorporation for hafnium oxide and

[1] From now on, HfN or HfON will be used through the dissertation instead of Hf_xN_y and HfO_xN_y just for simplicity.

hafnium silicate films. According to M.R. Visokay's report [38], incorporation of both Si and N into HfO_2 is inevitable to increase crystallization temperature and avoid phase separation at CMOS processing temperature. However, dielectric constants are reduced in HfSiON due to the presence of silicon oxide bonds with much lower dielectric constant than HfO_2. According to a report [39], HfSiON with optimized composition remained amorphous state up to 1100℃ whereas dielectric constant decreased down to ~10. In terms of application, the HfSiON appears to be very promising materials for the low power devices rather than high speed device requiring further scaling-down of EOTs < 10Å in the near future.

In contrast, HfON appears to be promising for further scaling-down of EOT since incorporated nitrogen does not degrade dielectric constant of the film. In addition, HfON is formed by very simple process: deposition of HfN followed by post-deposition-anneal (PDA) with the same process steps as in the HfO_2 films. Except interface quality that might be degraded by the presence of nitrogen, HfON films are expected to have advantages in achieving the requirements for the MOSFET application compared to top nitridation, surface nitridation, and HfO_2. HfON has a merit in the thermal stability compared to surface nitrided and top nitrided HfO_2 because nitrogen bonds exist in the bulk-dielectric as well as at the dielectric/Si interface. Although it crystallizes around ~800℃ [41] not high enough to remain amorphous phase in the conventional self-aligned source/drain process, it provide higher scalability than HfSiON due to its higher dielectric constant (~21). Therefore, it is worth further studying on the electrical and material characterization of HfON film. In this work, a comparative study on metal-oxide-semiconductor (MOS) characteristics of HfON and HfO_2 were mainly focused on and the differences were discussed in relation to material analysis. Also, efforts were made to understand the role of nitrogen and silicon in the Hf-based dielectrics.

1.4 OUTLINE

Hf is a new material which has never been used in the conventional CMOS process. Thus, the effect of cross-contamination of Hf on the other device properties should be accessed before it is introduced into the product line. Chapter 2 covers the effect of Hf introduced to SiO_2 based MOS capacitor and MOSFETs.

Electrical properties of Hf-based dielectrics in this work were characterized using TaN gates. The dielectric property is also dependent on the type and fabrication process of gate electrodes. In chapter 3, gate electrodes for high-k materials are reviewed and electrical properties of TaN gate electrode as a potential metal electrode for high-k materials are described.

Chapter 4 will point out several issues in HfO_2 dielectrics from a perspective of application into CMOS process. As an approach to improve a demerit of pure HfO_2: insufficient thermal stability, surface nitridation technique is studied in chapter 4.

Chapter 5 presents fabrication procedures of nitrogen incorporation techniques and material properties of HfON films. In chapter 5, the technique was realized by PVD deposition and optimization of post-deposition annealing.

Chapter 6 deals with the performance and reliability of HfON-MOSFET transistors with TaN metal gates. In chapter 6, properties of HfON dielectrics will be investigated and discussed in the prospect of a point of device applications.

Device characteristics of HfON film are dependent on the nitrogen profile as well as nitrogen concentration. In chapter 7, the nitrogen profile in the HfON films were modulated by inserting Si layers. Then, the effects of nitrogen profile on the device characteristics and reliability are investigated.

Finally, chapter 8 will summarize this work and suggest future research in this area.

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Chapter 2: Effects of Hf contamination on the properties of silicon oxide MOS devices

2.1 MOTIVATION

High dielectric (high-k) materials such as HfO_2 [1], ZrO_2 [2], their silicates [3], and nitrides [4], have received much attention for gate dielectric application to replace the conventional thermal silicon oxide which has higher leakage current and reliability problems < 20 **Å** regime [5]. Among high-k materials, hafnium-based dielectrics showed compatibility both for polycrystalline Si and metal gate process in the ultrathin EOT regimes. Introduction of Hf or Zr into the Si based complimentary metal-oxide-semiconductor (CMOS) may cause a concern because the out-diffusion of the metals can degrade device performance [6]. It is well known that impurity out-diffusion into the channel regions would likely result in deleterious effects such as impurity-induced breakdown [7], and degradation of carrier mobility [8]. Quevedo-Lopez et al. [8] reported that surface concentration of hafnium diffused from $(HfO_2)_{1-x}(SiO_2)_x$ layer into the Si substrate amounted $4x10^{10}/cm^2$. Hegde et al. investigated the effect of Hf contamination on the minority carrier lifetime that is a valuable parameter for the level of cleanliness and contamination of a silicon wafer [6]. However, there have been very few reports on effects of the metal contaminations from high-k dielectrics on the properties of the silicon-based MOS devices.

In this chapter, the effects of Hf contamination into the Si substrate on the electrical properties of MOS capacitors and electron mobility of n-MOSFETs were investigated using a structure of n-type polycrystalline-Si/SiO_2/p-type Si substrate. In order to ensure accurate counting of Hf ions, ion implantation was used to introduce Hf ion into the Si substrate. Capacitance-voltage (C-V) curves and leakage current

characteristics of the capacitors with various doses of Hf were compared to those of control samples without intentional Hf contamination. Electron channel mobility was measured using nMOSFETs fabricated by conventional self-aligned CMOS process [9].

2.2. EXPERIMENT

Field oxide films (~3000 **Å**) grown on p-type (100) Si substrates with a resistivity of 5~25 Ωcm were patterned to define capacitor areas. Then, 370-**Å**-thick oxide film was thermally grown as a pad layer to prevent implant damage and to adjust projected range (R_p) of Hf implantation. Hf was implanted into the Si substrate through the pad oxide layer with various doses. Table 2.1 shows the implantation conditions for this work. Implantation energy was 80 keV. With the implantation energy of 80 keV and the pad oxide thickness, R_p was placed at the interface between the pad oxide layer and the Si substrate. Doses were varied from $1x10^{11}/cm^2$ to $1x10^{13}/cm^2$. The lower limit of the dose is ten times larger than ~ $1x10^{10}/cm^2$, the typical allowable amount of metal contamination in ULSI environment [10]. The upper limit of the dose, $1x10^{13}/cm^2$ is sufficiently larger than ~$5x10^{10}/cm^2$, the amount diffused into the Si substrate by a feasible HfO_2 gate dielectric formation process and contamination level developed by dry etch procedures (~ 1 $x10^{10}$ ~ 1 $x10^{11}$ metals/cm^2) [11].

After the Hf implantation, the samples were annealed at 950 ^oC in nitrogen ambient for 1 min to eliminate the implantation damages. The pad oxide layer was stripped by buffered oxide etchant (BOE) and subsequently cleaned by SC-2 solution (H_2O:HCl:H_2O_2=5:1:1), to remove residual heavy metal contaminants. As a capacitor dielectric, 50~55 **Å** -thick oxide film was then immediately grown on the cleaned Si substrate at 950 ^oC in oxygen ambient by rapid thermal oxidation (RTO). As gate electrodes, polycrystalline Si films (~1700 **Å**) were formed at 580 ^oC by chemical vapor

deposition using SiH_4 as a source gas and patterned to define gate electrodes. Subsequently, the samples were implanted by phosphorous with $5x10^{15}/cm^2$ of dose and 50 keV of energy, and activated at 980 ^oC for 1 min. Before measurements of capacitor characteristics, Al was deposited on the backside of the samples to ensure lower contact resistance between substrate and measurement probe. C-V curves and transistor characteristics were measured by a HP 4194 LCR meter and a HP 4156, semiconductor parameter analyzer, respectively. The area of the capacitor was $5x10^{-5}cm^2$.

	Ion species	Energy (keV)	Rp (Å)	Dose (atoms/cm^2)
1	Hf	80	380	$1x10^{11}$
2	Hf	80	380	$1x10^{12}$
3	Hf	80	380	$1x10^{13}$
4	control sample without Hf implantation			

Table 2.1 Implant conditions of Hf into thermally grown pad oxide (~380Å)/Si substrate.

2.3 RESULTS AND DISCUSSIONS

The high-frequency (1 MHz) C-V curves show typical well-behaved MOS capacitor characteristics (Fig. 2.1). The discrepancies in maximum capacitance (C_{max}) between the samples come from run-to-run variations of the RTO oxide ranging from 50 to 55 **Å**, not from the variations in various implantation conditions. The dependency of RTO oxidation rate on the implantation conditions seems to be negligible. There cannot be seen any other distinguished differences among the C-V curves. The extracted flat band voltage (V_{fb}) and substrate doping concentration (N_A) from C-V characteristics can be used to determine whether Hf is active in the Si substrate.

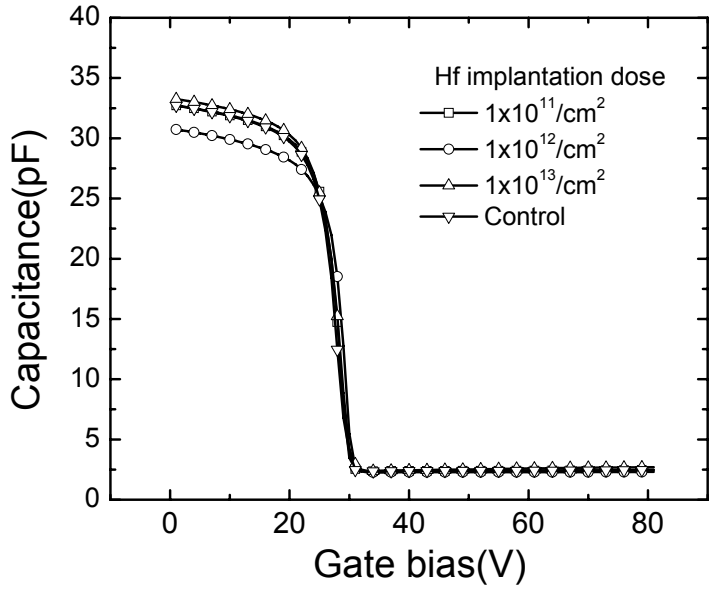

Figure 2.1 C-V curves for n^+ polycrystalline-Si/SiO_2/p-type Si capacitors with different doses of Hf implanted into the Si substrate

Figure 2.2 shows that there is no dependence of N_A on the implantation doses of Hf. The V_{fb} values are larger compared to expected V_{fb} (~0.85 V) for the MOS capacitor with n^+ polycrystalline-Si gate and the substrate doping concentration in the figure. This fact appears to be caused by larger fixed charge density ($\cong 1x10^{11}/cm^2$) in the RTO silicon oxide used in this experiment. However, the variation of V_{fb} with varying implantation condition is negligible, and the V_{fb} value is similar to that of the control sample.

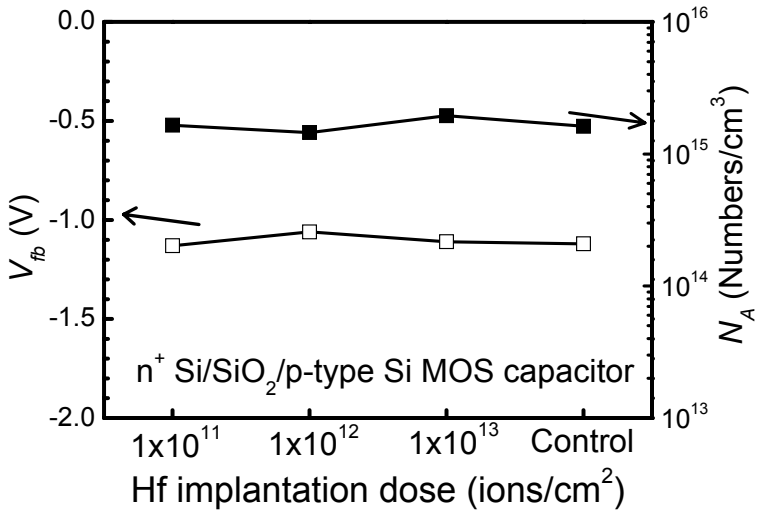

Figure 2.2 N_A and V_{fb} values of n^+ polycrystalline-Si/SiO_2/p-type Si MOS capacitors as a function of Hf implantation dose. The values were extracted from high frequency C-V curves.

Figure 2.3 shows leakage current density vs. gate bias voltage (J-V) curves. The J-V curves were measured in the accumulation region. While a capacitor with a Hf dose of $1x10^{13}/cm^2$ shows slightly higher leakage current level probably due to damages from the higher dose of the implantation, J-V curves are nearly the same for the other samples. This result agrees with a report that Hf contamination levels developed during dry etch procedures (~ $10^{11} – 10^{12}$ metals/cm^2) had no significant effect on device parameters such as C-V, J-V and time dependent dielectric breakdown (TDDB) [11]. From the observation on N_A, V_{fb}, and J-V curves, it can be concluded that the level of Hf contamination in this work has negligible effects on the electrical properties of the silicon oxide capacitor.

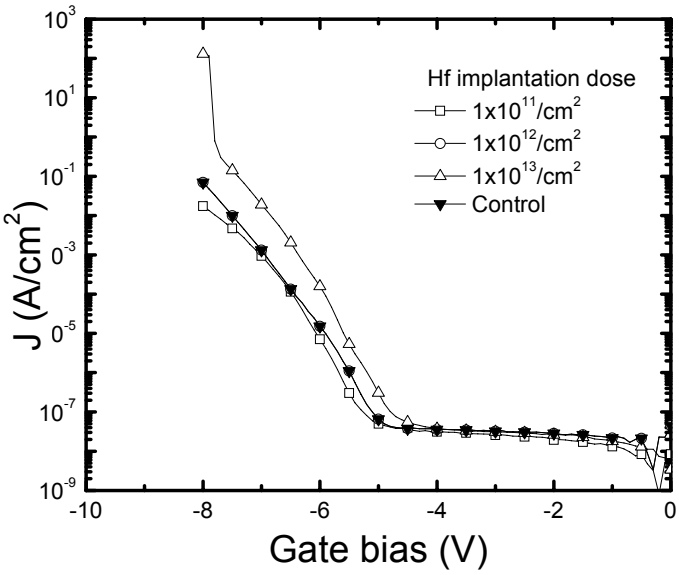

Figure 2.3 Comparison of J-V curves for MOS capacitors with different Hf implant with a control capacitor for different Hf doses.

Figure 2.4 compares electron channel mobility of MOSFETs with 45-**Å**-thick silicon oxide as gate dielectrics as a function of effective field for silicon substrates implanted by Hf with doses of $1x10^{10}/cm^2$ and $1\ x10^{11}/cm^2$ and a control sample without an intentional Hf contamination. The gate length (L) and width (W) of the devices were 10 μm and 150 μm, respectively. The electron mobility was calculated from drain current-gate bias (I_d-V_g) curve and gate to channel capacitance (C_{gc}) vs. V_g curves (not shown here) of the MOSFETs using a well-known equations (2.1) ~ (2.3) [11].

Effective mobility of carrier can be expressed by a simple equation (2.1),

$$\mu_{eff}(V_g) = \frac{I_d / V_d}{(W/L)Q_{inv}(V_g)} \qquad (2.1)$$

where $\mu_{eff}(V_g)$ and $Q_{inv}(V_g)$ represent effective mobility and inversion charge density as a function of gate voltage, respectively. If gate to channel capacitance (C_{gc}) is measured as a function of gate voltage, then $Q_{inv}(V_g)$ is calculated from an integration of the C_{gc} for V_g from accumulation regions to V_g by equation (2.2). In addition, effective field E_{eff} is a function of inversion charge and depletion charge (Q_D) with a relationship of equation (2.3).

$$Q_{inv}(V_g) = \int_{-\infty}^{V_g} C_{gs}(V_g)dV_g \qquad (2.2)$$

$$E_{eff} = \frac{(0.5Q_{inv} + Q_D)}{\varepsilon_{Si}} \qquad (2.3)$$

In Fig. 2.4, the peak mobility of the Hf-contaminated sample (470 ~480 cm^2/Vsec) appears to be comparable to that of the control sample (470 cm^2/Vsec). The result indicates that Hf incorporation has little effects on the channel electron mobility compared with a control device.

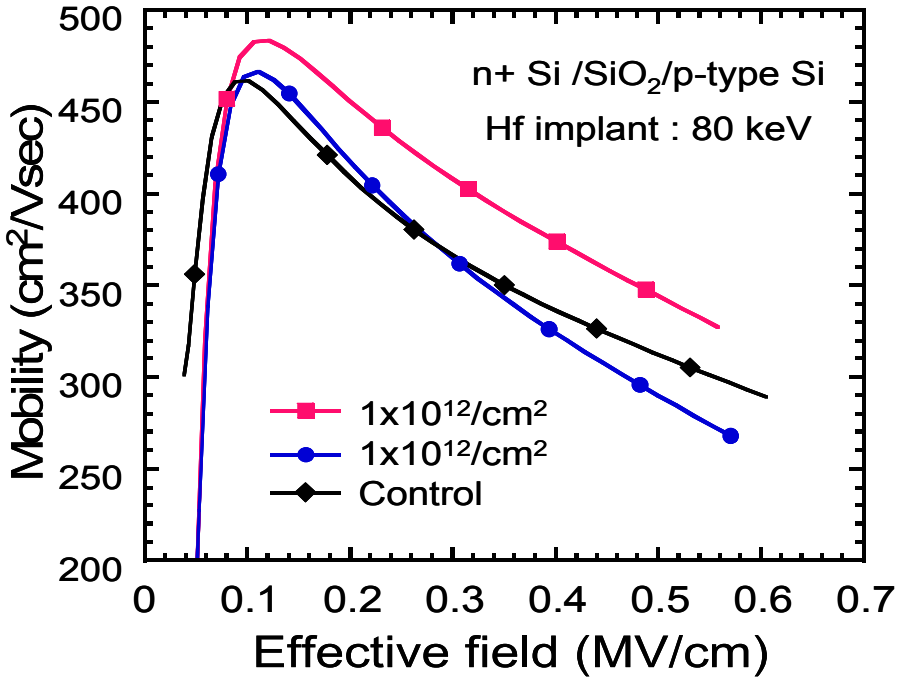

Figure 2.4 Effects of intentional Hf incorporation on the channel electron mobility of nMOSFETs.

2.4 CONCLUSIONS

The effects of Hf implanted into p-type Si substrates on the properties of n^+ polycrystalline-Si/SiO_2/Si capacitors and MOSFETs have been investigated. Flat-band voltages (V_{fb}) and substrate doping concentrations (N_A) calculated from high frequency C-V curves of the capacitors was not dependent on the doses of Hf. Leakage current density of the MOS capacitor was also negligibly affected by the implant condition. Also, electron channel mobility was not degraded by Hf contamination. Therefore, one can conclude the amount of Hf diffused into Si substrate during the high-k dielectric impose negligible effects on silicon based MOS device characteristics.

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Chapter 3: Characterization of resistivity and work function of sputtered-TaN film for gate electrode applications

3.1 MOTIVATION

As complimentary metal oxide semiconductor (CMOS) devices are scaled down to 100 nm technology node or beyond, ultra-thin gate dielectrics with equivalent oxide thickness (EOT) less than 15 Å are needed [1]. High dielectric (high-k) materials such as HfO_2 [2], ZrO_2 [3], their silicates [4] and nitrides [5] have received much attention. In the ultra-thin EOT regimes, the conventional poly-Si gate electrode has concerns due to its limitations: poly-Si depletion effects and dopant penetration effects [6]. An obvious way to alleviate the problems of poly-Si is adopting refractory metal or metal-nitride gates. The requirements for the advance gates are as follows: a) favorable work functions b) low sheet resistance c) thermal stability and d) compatibility with high-k dielectric and integration technology [7]. In Fig. 3.1, work functions of metal gate electrodes from various reports were summarized. Among the proposed advanced gate electrodes, TaN gates showed promising results as the gate electrodes for the high-k gate dielectrics in thermal stability and compatibility with the high-k gate dielectrics [8].

Although TaN thin film has been studied widely for many applications [9] such as thin film resistors, write-head materials for magnetic recording, wear-resistant coatings on tools, thermal printer heads (TPH), and diffusion barrier layers in Cu interconnection, there have been few reports on the systematic study for the application to the gate electrodes. Besides, there exists a significant variance in reported work functions of TaN varying from 4.13 eV (similar to that of n^+ poly-Si) to 5.05 eV (similar to that of p^+

poly-Si) [10]. In addition, Park et al. reported that the work function of TaN was 4.5 eV, closer to mid-gap of silicon [11]. Those discrepancies may be attributed to the differences in nitrogen atomic ratio in TaN films, thermal processes after TaN deposition, and formation methods. In this letter, sheet resistance, crystalline structure and work function of TaN film were studied as a function of nitrogen flow rate in reactive sputtering and post-metal annealing (PMA) conditions for the gate electrode application.

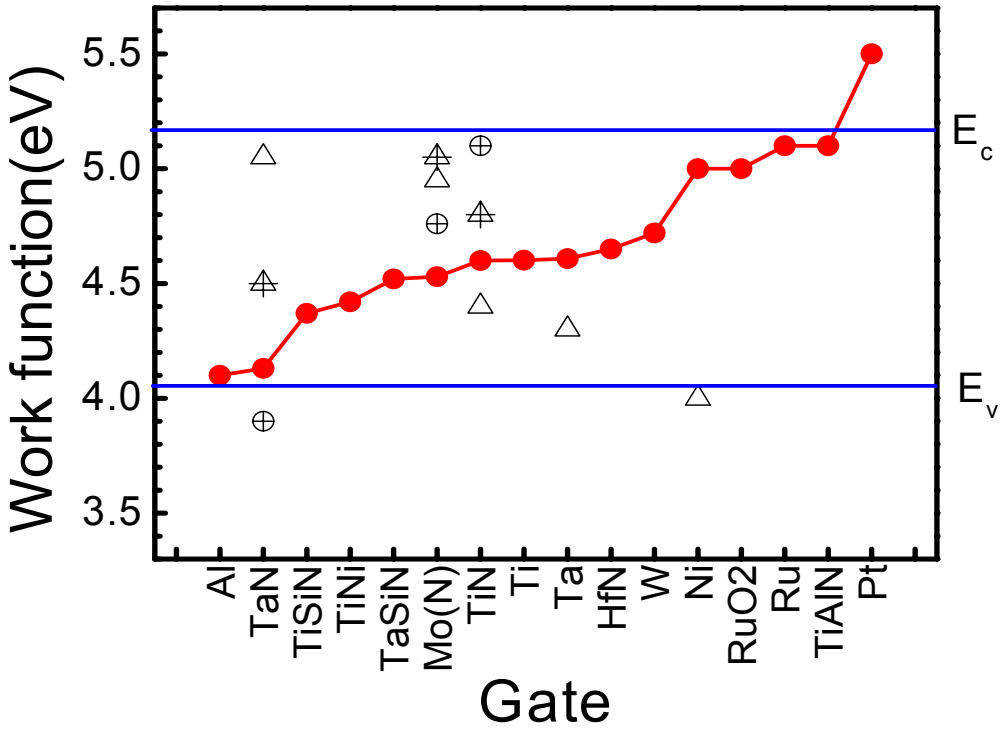

Figure 3.1 Work functions of metal gate electrodes. The reported value shows a wide variation probably stemming from different fabrication technique, condition, and post-deposition annealing. The data were collected from various reports. (1.TED 48, p.1604, 2001; 2. EDL 23, p.49, 2002; 3. IEDM 95, p.881, 1995; 4. EDL 24, p. 550, 2003; 5. IDEM 00, p.28.2.1, 2000; 6. IEDM 01, p.671, 2001; 7. EDL 24, p.230, 2003; 8. VLSI 90, p.115, 1990; 9. IEDM, 30.5.1, 2001; 10. EDL 21, p.593, 2000; 11. EDL 23, p.354, 2002)

3.2 EXPERIMENT

To investigate the material properties of TaN films, 2000-Å-thick film was reactively sputtered on thermally grown 3500-Å-thick SiO_2/Si (100) substrates by magnetron sputtering. Ar and N_2 were used as sputtering gas with varying nitrogen flow rates from 0 to 20 sccm and a fixed Ar flow rate (20 sccm). The sputtering chamber was pumped down below $5x10^{-7}$ Torr prior to every deposition. Sputtering power density and chamber pressure were fixed at 6 W/cm^2 and 10 mTorr, respectively. No intentional substrate heating was performed. After the deposition of TaN films, some films were annealed in nitrogen ambient to investigate the thermal behaviors of sheet resistance and work function. Sheet resistance was measured by four-point probe. Crystalline structures of the films were measured using a glancing angle X-ray diffractometer (XRD) with a Cu K_α source.

TaN-gated nMOS capacitors with SiO_2 gate dielectrics were adopted to evaluate work function of TaN films. The SiO_2 dielectrics with thickness ranging from 28 to 44 Å were grown on p-type (100) Si wafer cleaned by dilute HF solution using rapid thermal oxidation (RTO) at 950^{o}C in 1 atm. After growing the SiO_2 dielectrics, 2000-Å-thick TaN gate was sputtered. The TaN gates were patterned by reactive ion etching (RIE) using CF_4 as an etch gas. Subsequently, backside-Al deposition and forming gas annealing were performed. The work function of TaN film was calculated from a relationship between a flat band voltage (V_{fb}) and SiO_2 thicknesses (t_{ox}). V_{fb} was extracted from the capacitance-voltage (C-V) curves measured by HP4194A LCR meter. The area of the capacitor was $5x10^{-5}$ cm^2.

3.3 RESULTS AND DISCUSSION

Figure 3.2 shows the dependency of TaN resistivity on the nitrogen flow rate during the sputtering. The resistivity was obtained from the measured sheet resistance (R_s) x TaN thickness (t) measured by a surface profiler. With increasing nitrogen flow rates from 0 to 20 sccm, the resistivity of TaN_x increased from 132 to $1.4x10^5$ μΩcm for as-deposited film; and from 135 to $2x10^3$ μΩcm after post-metal anneal (PMA) at 950°C for 1 min under nitrogen ambient. It can be seen that PMA had little effects on the resistivity of the film except for the nitrogen flow rate of 20 sccm. That is, the resistivity of TaN is quite stable after high-temperature annealing. It appears that TaN films with nitrogen flow rate of 20 sccm and 0 sccm (pure Ta) are not favorable since the former resulted in high and the latter can oxidize easily in oxidation ambient.

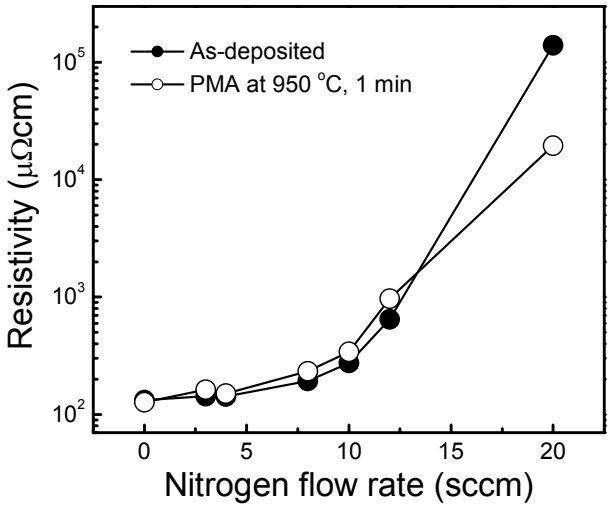

Figure 3.2 Resistivity of TaN films as a function of nitrogen flow rate at a fixed Ar flow rate (20 sccm) during the sputtering. The films were deposited on the SiO_2/Si substrate under 10 mTorr and a sputtering power of 6.0 W/cm^2. Post-metal anneal (PMA) was performed at 950^{o}C for 1 min under N_2 ambient.

The XRD spectra of 2000-Å-thick TaN films on SiO_2/Si substrate with various nitrogen flow rates are shown in Fig. 3.3. When no nitrogen was added in the sputtering chamber, there appeared (200) peak of β-Ta phase. As the nitrogen flow rate increased, the phase of the film evolved from Ta to TaN. For nitrogen flow rate of 8 and 10 sccm, sharp (111) and (200) peaks of face-centered cubic (fcc) TaN were observed. The decreased peak intensity of TaN for the nitrogen flow rate > 12 sccm indicates that for higher nitrogen concentration led to a much smaller polycrystalline TaN grains with random orientation. Although N-rich phase are not present in the XRD spectra, the increased resistivity in the TaN film with nitrogen flow rate > 12 sccm indicate existence of N-rich phase in the TaN film [12].

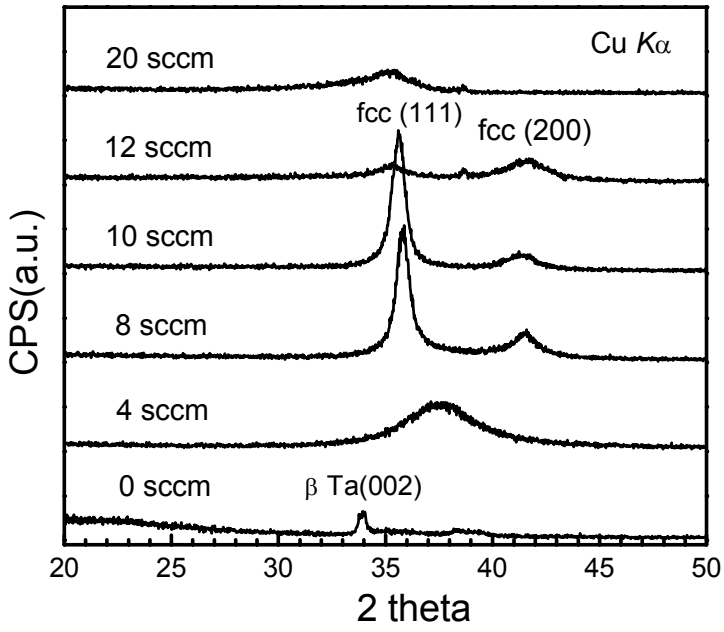

Figure 3.3 XRD spectra showing crystalline structure of TaN film on SiO_2/Si substrate as a function of nitrogen flow rate.

Flat bands (V_{fb}) of TaN-gated MOS capacitor are plotted against SiO_2 thickness for before and after PMA at 950 ^{o}C for 1 min in Fig. 3.3 (a-b). The y-intersection and the slope in Fig. 4 correspond to (ϕm - ϕs) and Q_f, respectively, from equation (3.1) [13].

$$V_{fb} = (\phi_m - \phi_f) - \frac{Q_f t_{ox}}{\varepsilon_{sio_2}} \qquad (3.1),$$

where ϕ_m, ϕ_s, Q_f, t_{ox}, and ε_{sio_2} are work functions of gate electrode, the Fermi level of the Si substrate, fixed charge density, SiO_2 thickness, and dielectric constant of SiO_2, respectively. Steeper positive slopes indicating negative fixed charge in the dielectric were observed for the TaN-gated MOS capacitors without PMA in Fig. 3.4 (a).

In contrast, gentle negative slopes were shown in the capacitors after PMA (Fig. 3.4 (b)). The ϕ_s for the p-type substrate (N_A~ 2x10^{15}/cm^3) is 4.9 eV.

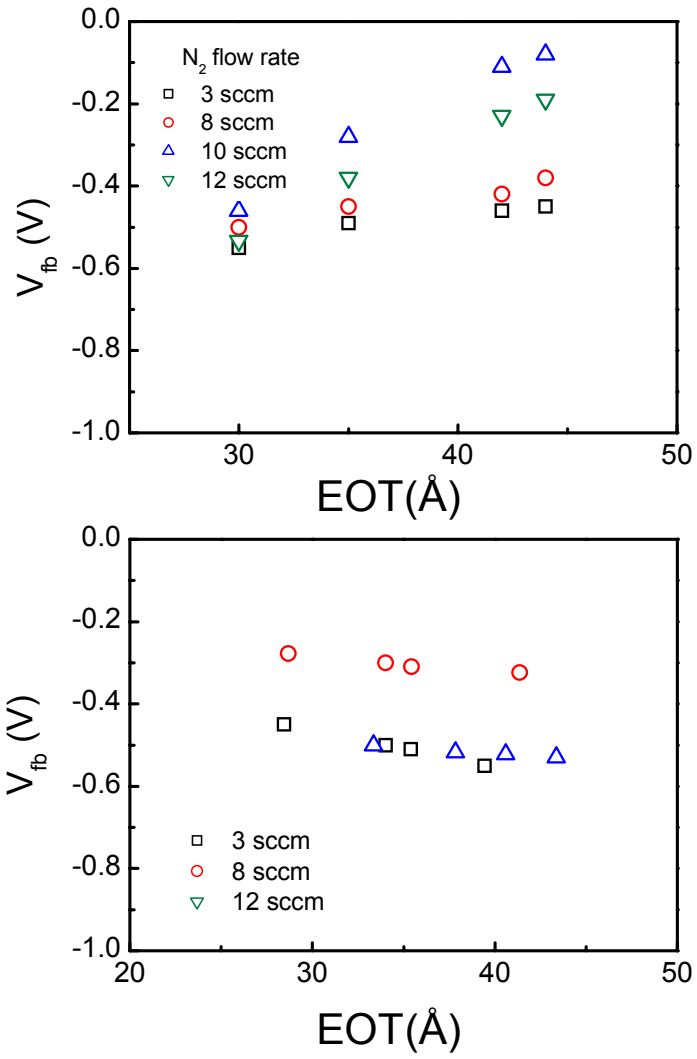

Figure 3.4 Flat band variation as a function of SiO_2 thickness in TaN-gated MOS capacitors before (a) and after PMA at 950 ^oC for 1 min under N_2 ambient.

Figure 3.5 shows work functions of TaN films as a function of nitrogen flow rate before and after the PMA at 950 ^{o}C. Without the PMA, TaN films deposited using nitrogen flow rates of 4 sccm and 8 sccm exhibited similar work functions of ~ 4.15 eV, whereas N_2 rates of 10 sccm and 12 sccm resulted in ϕ_m's of 3.6 eV and 3.7 eV, respectively. After PMA at 950 ^{o}C for 1 min, the work functions increased to 4.5 eV to 4.7 eV, with less dependency on the nitrogen flow rate. The obtained work functions after PMA appear to be closer to silicon mid-gap than the results by Park et al. [11], while smaller than the reported work function of TaN prepared by CVD [10].

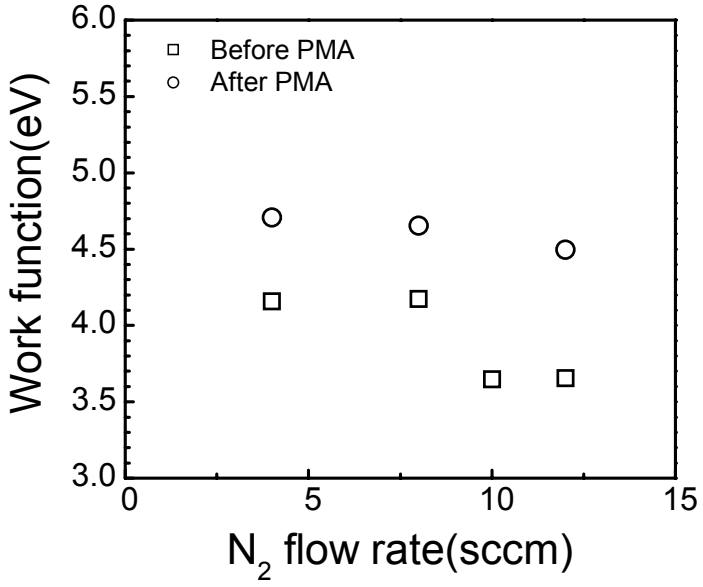

Figure 3.5 Work function variation as a function of nitrogen flow rate before and after PMA at 950 ^{o}C for 1 min under N_2 ambient.

3.4 SUMMARY

Tantalum nitride (TaN) film was prepared by reactive sputtering in Ar/N_2 ambient for gate electrode application. Resistivity, crystallinity and work function of TaN film were investigated as a function of nitrogen flow rate. As nitrogen flow rate increased from 0 to 20 sccm, the resistivity of as-deposited TaN film increased from 132 to $1.4x10^5$ Ω cm. With nitrogen flow rate of 8 and 10 sccm, fcc-TaN phase were obtained. Work function of TaN film was investigated using TaN-gated nMOS capacitors with SiO_2 gate dielectrics of various thicknesses. As nitrogen flow rate increases from 4 to 12 sccm, work function decreased from 4.1 eV to 3.4 eV for as-deposited films. After annealing at 950 ^oC for 1 min, the work functions increased to 4.5 eV ~ 4.7 eV, with less dependency on the nitrogen flow rate.

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Chapter 4: Scaling down of ultrathin HfO_2 gate dielectrics by using nitrided Si surface

4.1 MOTIVATION

High dielectric constant (high-k) materials such as HfO_2 [1], ZrO_2 [2], their silicates [3, 4] and nitrides [5, 6] have been under intense investigation for gate dielectric application into the 70 nm technology nodes and beyond to replace conventional SiO_2 or oxynitrides because of the excessive leakage current and reliability concerns. Among the potential materials, HfO_2 showed compatibility both for polycrystalline Si [7], poly-SiGe [8] and TaN gates [9] process in the ultra-thin equivalent oxide thickness (EOT) regimes.

MOSFETs with HfO_2 dielectrics and TaN gate showed very low EOT (~10 Å) and low leakage current even after the conventional CMOS process flow [9]. Considering the cost of development and implementation, HfO_2 gate dielectric needs to span two or three generations in 70 nm to 35 nm design rule. To meet this requirement for the generations, EOT should be scaled down to 10 Å while suppressing leakage current to below 1 A/cm^2 [10]. In the range of EOT < 10 Å, metal gate is more attractive than poly-Si gate because the poly-Si depletion effect can be avoided. However, further scaling of EOT below 10 Å seems to be difficult without using a replacement gate process because EOT increase due to the formation of an interfacial layer between HfO_2 and Si at high temperature [11]. The EOT increase during PMA would limit the use of high-k dielectrics for the self-aligned gate process requiring high temperature thermal process after the transistor fabrication.

Even for processes without post-metal annealing (PMA), there exists an interface layer (~5 Å), which is presumed to be hafnium silicate formed during reoxidation step [12]. Therefore, to scale down HfO_2 for the 100 nm devices, it is necessary to reduce interfacial layer formation by a surface preparation. In this respect, nitridation of Si surface is effective because the nitrided layer has higher dielectric constant and lower oxygen diffusion [13].

The potential drawbacks of the nitridation technique are increase in the interface state density and fixed charge density [14]. The interface charge (D_{it}) and fixed charge degrade not only channel mobility but also uniformity of threshold voltage of MOSFET devices [15]. Thus, interfacial quality of nitrided devices is of concern and should be addressed.

In this chapter, Si surface nitridation technique using NH_3 anneal has been investigated to further scale down EOTs of HfO_2 gate dielectrics. Previous studies showed that the nitridation technique provides some improvements on device characteristics [16, 17]. However, there have not been systematic studies on the effect of nitridation in MOSCAP devices with HfO_2 gate dielectric, especially, on the interface qualities of the nitrided surfaces for the capacitor with TaN gate. In addition, We comparison of interface states and hysteresis in capacitance-voltage (C-V) curve of the HfO_2 gate dielectric were made between nitrided and non-nitrided Si surfaces.

4.2. EXPERIMENTAL PROCEDURES

Metal oxide semiconductor (MOS) capacitors with HfO_2 dielectrics were fabricated on (100) p-type silicon wafers with resistivities of 5~25 Ωcm. Active regions with an area of $5x10^{-5}$ cm^2 were defined using patterned field oxide. The active patterned wafers were cleaned using 100:1 HF. Without time delay, the surface of Si wafers was

annealed using rapid thermal anneal (RTA) in NH_3 ambient at 760 Torr. The anneal temperatures and times were varied from 500°C to 800°C and from 10 sec to 60 sec, respectively. After nitridation, metal Hf was deposited at room temperature by dc magnetron sputtering and followed by annealing at 600°C for 40 sec under a N_2 ambient with a trace amount of oxygen (~10 ppm) using RTA [9]. The physical thickness of HfO_2 measured by a single wavelength ellipsometer was about 50 Å. As a gate material, 2000-Å- thick TaN gate was deposited by reactive dc sputtering at 10 mTorr of chamber pressure using Ar and N_2 as sputtering gases. Sheet resistance of the TaN film was approximately 10 Ω/square. The TaN gate was patterned by reactive ion etch using CF_4 mixture as etching gas. Post-metal anneal (PMA) in nitrogen ambient was done for some samples to investigate thermal stability of the capacitor.

Capacitance (C) and leakage current density (J) were measured at the frequency at 1 MHz using a HP4194A LCR meter and a HP4156 semiconductor parameter analyzer, respectively. D_{it} was extracted using the capacitance difference between measurement at 1 MHz and ideal values at the depletion region (Terman method [18]).

4.3 RESULTS AND DISCUSSION

Figure 4.1 (a) shows the dependence of EOT and leakage current density on the nitridation temperature for the TaN/HfO_2(50Å)/Si MOS capacitor. There exists optimum nitridation temperature range (600~700 ^oC) to obtain reduced EOT. The increase of EOT at 800 ^oC can be attributed to the oxidation of the Si surface due to the residual oxygen in nitridation chamber or NH_3 gas. It is well-known that purity of NH_3 gas is very important factor to suppress undesired oxidation of Si surface in the nitridation of Si [19]. In this experiment, vacuum pump was not attached in the RTA, thus residual oxygen or impurity oxygen in the NH_3 gas may cause the oxidation of Si

surface at higher temperature. The effect of nitridation time on the capacitor properties was negligible as shown in Fig.4.1 (b).

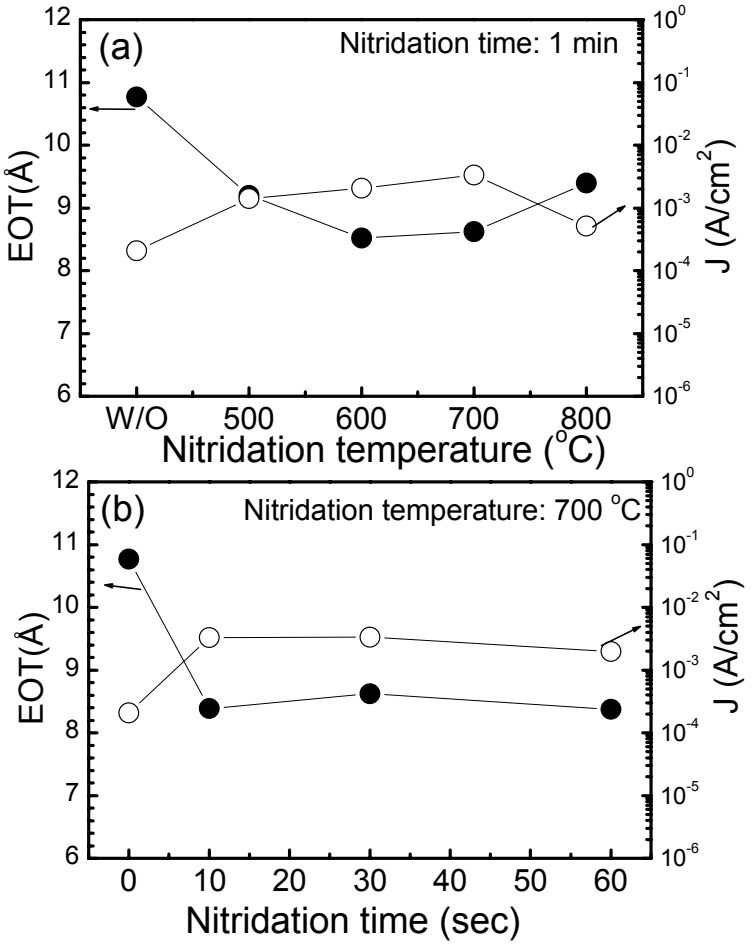

Figure 4.1 Variation of EOT and leakage current density (J) measured at –1.5V as a function of nitridatoin temperature for 50 Å -thick HfO_2 gate dielectric. The nitration time was 30 second. The inset is the variation of EOT and J as a function of nitridation time.

J measured at –1.5V is plotted against EOT in Fig.4.2. For the same EOT, nitrided samples show 1 ~ 2 orders of magnitude smaller leakage current density compared to non-nitrided ones. The improvement in EOT and leakage current by the NH_3 surface annealing can be attributed to very thin nitrided layer formed during NH_3 RTA process. Existence of the nitrided layer was confirmed by XPS analysis [20]. It is believed that this nitrided layer blocks the diffusion of oxygen and prevents the excessive interfacial layer growth.

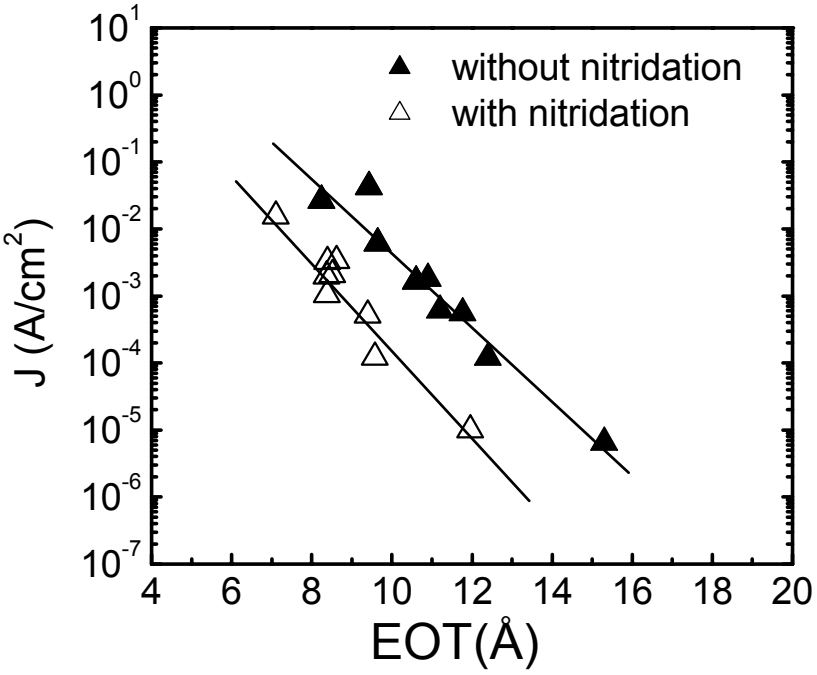

Figure 4.2 Leakage current density (J) measured at –1.5V as a function of EOT.

Variation of EOT change as a function of post-TaN annealing temperature is depicted in Fig. 4.3. The initial EOT was ~10 Å . TaN was reported to have good thermal stability from a point of view of sheet resistance [21]. However, EOT increases due to the growth of the interfacial layer during the subsequent process. As shown in Fig. 4.3 for the non-nitrided samples, there was a significant increase in the EOT values (ΔEOT ~ 3.2 Å after 1 min 900 ℃ anneal). In contrast, the increase in EOT for nitrided sample was less than 1.5 Å.

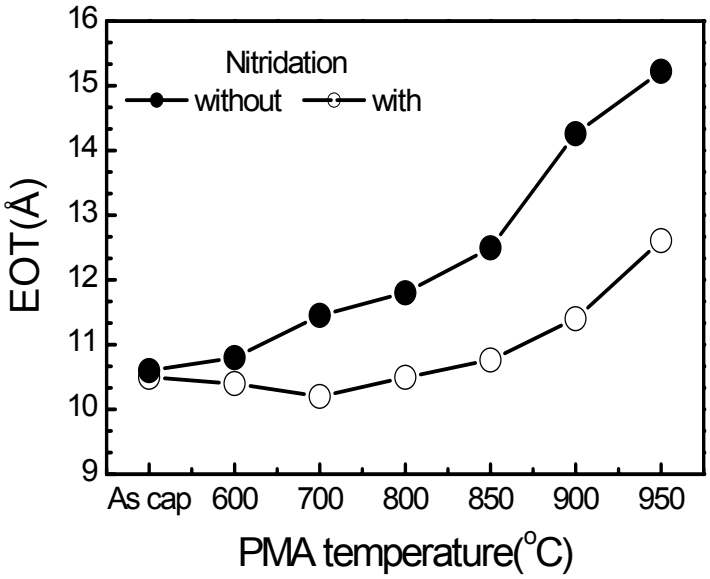

Figure 4.3 Variation of increased EOT by the thermal budget during the subsequent process after patterning TaN gate as a function of RTA. RTA time was 1 minute.

High-resolution transmission electron microscopy (HR-TEM) pictures were shown in Fig. 4.4 for the dielectric layers on Si substrates after PMA at 900°C for with and without nitridation. It is worth noting that the HfO_2 deposited on surface nitrided Si substrate shows thicker interface layer (IL) of 15Å than that of the dielectric without surface nitridation (10 Å). As mentioned before, the surface-nitrided capacitor showed reduced leakage current density with lower EOTs compared to the control samples. This result indicates that ILs of surface nitrided samples have higher dielectric constants than those of the control samples.

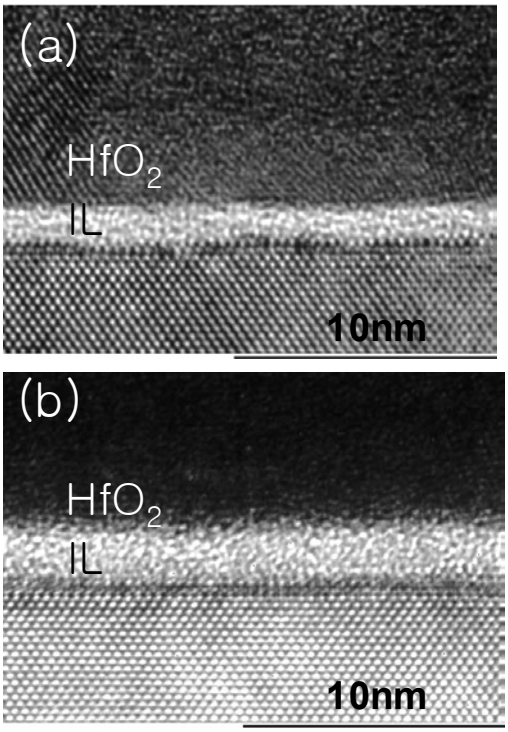

Figure 4.4 High resolution TEM pictures for the HfO_2 deposited on Si substrate with (a) without (b) surface nitridation. Interfacial layers of the dielectrics with and without surface nitridation were15 Å and 10 Å, respectively.

Figure 4.5 shows D_{it} at the mid-gap (at the surface potential=0) and EOT for four different groups: SN (**S**urface nitridation and **N**o PMA), SA (**S**urface nitridation and PM**A**), NN (**N**o surface nitridation and **N**o PMA), and NA (**N**o surface nitridation and PM**A**). Prior to PMA, D_{it} for the nitrided sample (SN) is ~ $1x10^{11}$ eV^{-1}/cm^2, larger than that of non-nitrided one (NN, $8.5x10^{10}eV^{-1}/cm^2$). With PMA, D_{it} of SA decreases to ~ $8.4x10^{10}$ eV^{-1}/cm^2, nearly the same value of NN, but still slightly larger than that of NA (~$6.2x10^{10}$ eV^{-1}/cm^2). All the obtained D_{it} values in Fig. 4.5 are reasonable compared with ~$2x10^{10}$ eV^{-1}/cm^2 for SiO_2/Si interface.

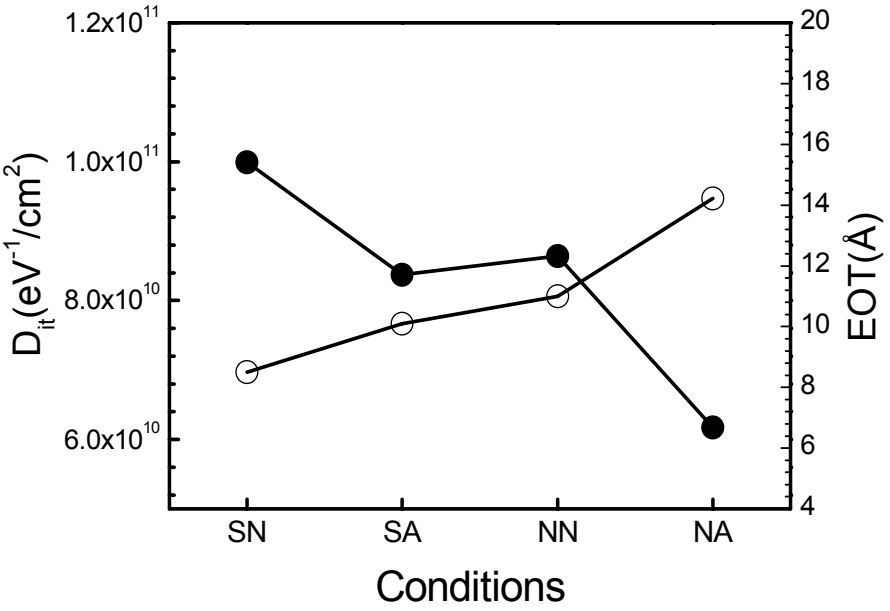

Figure 4.5 Variation of D_{it} for different sample group: SN (**S**urface nitridation and **N**o PMA), SA(**S**urface nitridation and PM**A**), NN (**N**o surface nitridation and **N**o PMA), and NA(**N**o surface nitridation and PM**A**).

Figure 4.6 (a) shows hysteresises as a function of PMA and nitridation condition. C-V curves for the nitrided sample are depicted in Fig.4.6 (b). Hysteresises of the nitrided sample (360 mV) are much larger than the non-nitrided ones (120 mV). However, with PMA, the hysteresise of the nitrided samples decreased significantly down to 45 mV, which is nearly the same value reported for poly-Si/HfO_2 devices [7]. Even though the hysteresis value after PDA for the nitridation meets the specification of V_{th} variation, ±34 mV (3σ) [22], further improvement in the interface quality of the nitrided films is demanded.

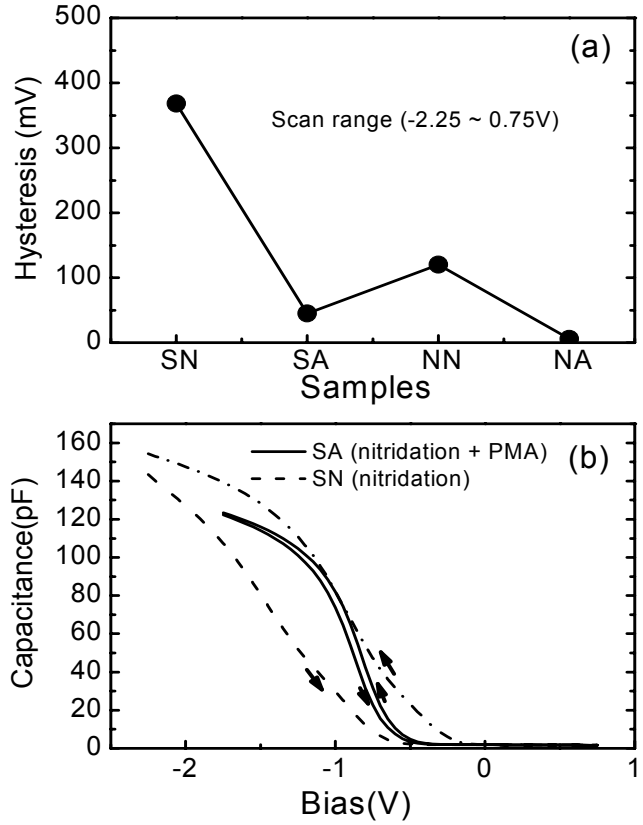

Figure 4.6 (a) Variations of hysteresis measure at the mid-value of capacitance for 4 different sample groups. Voltages was scanned from –2.25V to 0.75V. (b) C-V curves showing hysteresis for the nitrided samples with PMA (SA) and without PMA (SN). The EOTs for SA and SN correspond to ~10 Å and 8.1 Å, respectively.

4.4. SUMMARY

Surface nitridation technique using NH_3 anneal has been investigated to reduce interface reaction and consequently the equivalent oxide thickness (EOT) of TaN/HfO_2/ Si MOS capacitor. For the same EOT, the nitrided samples showed 1 ~ 2 order of magnitude lower leakage current density compared to the non-nitrided ones. Furthermore, the nitrided samples showed better thermal stability. However, nitridation induced higher interface state density and larger hysteresis. The degraded interface quality due to the nitridation was improved by post-metal annealing (PMA). Using the optimized nitridation and PMA, EOT of the capacitor was scaled down to ~10 Å with keeping leakage current below 0.1 mA/cm^2 at –1.5V. Interface state density (D_{it}) and hysteresis (ΔV) were ~$8.4x10^{10}$ eV^{-1}/cm^2, and 45 mV, respectively.

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Chapter 5: Nitrogen incorporated hafnium oxide (HfON): Process and Material Analysis[2]

5.1 FABRICATION PROCESS OF HfO_2 (HFON) MOSFETS

MOSFETs of TaN/HfO_2(HfO_xN_y)/Si and HfO_2 (HfO_xN_y)/Si were used for electrical characterization and chemical bonding analysis of the dielectric films, respectively. MOS capacitor and MOSFET fabrication process were detailed in Fig. 5.1. HfON[3] was formed by HfN[3] deposition using dc reactive sputtering with a 4-inch Hf (99.9% purity) target, followed by post-deposition annealing (PDA) to oxidize the HfN film. The HfN sputtering was performed in Ar+N_2 ambient (N_2/(Ar+N_2)=0.33) with discharging power density of 300 W and chamber pressure of 30 mTorr.

Deposition rates are compared for Hf and HfN film in Fig.5.2 as a function of sputtering power. HfO_2 as a control was fabricated by the same method detailed in chapter 4. Deposition rate of HfN is ~ 5 times slower than that of Hf deposition. The significant decrease in the deposition rate of HfN can be attributed to i) reduced plasma current due to the formation of more resistive HfN layer on the surface of the Hf target than metal Hf ii) difference in the sputtering yield between Hf and HfN. Fig. 5.3 shows that plasma current decreases linearly up to 8 sccm of nitrogen flow rate and then saturates at ~1.4 A as nitrogen is added into the discharging gas. From the plasma current vs. nitrogen flow plot, it can be inferred that the surface of the Hf target becomes fully nitrided at a nitrogen flow rate of ~8 sccm.

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[2] Motivation of the HfON was described in chapter 1.

[3] HfN or HfON will be used through the dissertation instead of Hf_xN_y and HfO_xN_y just for simplicity.

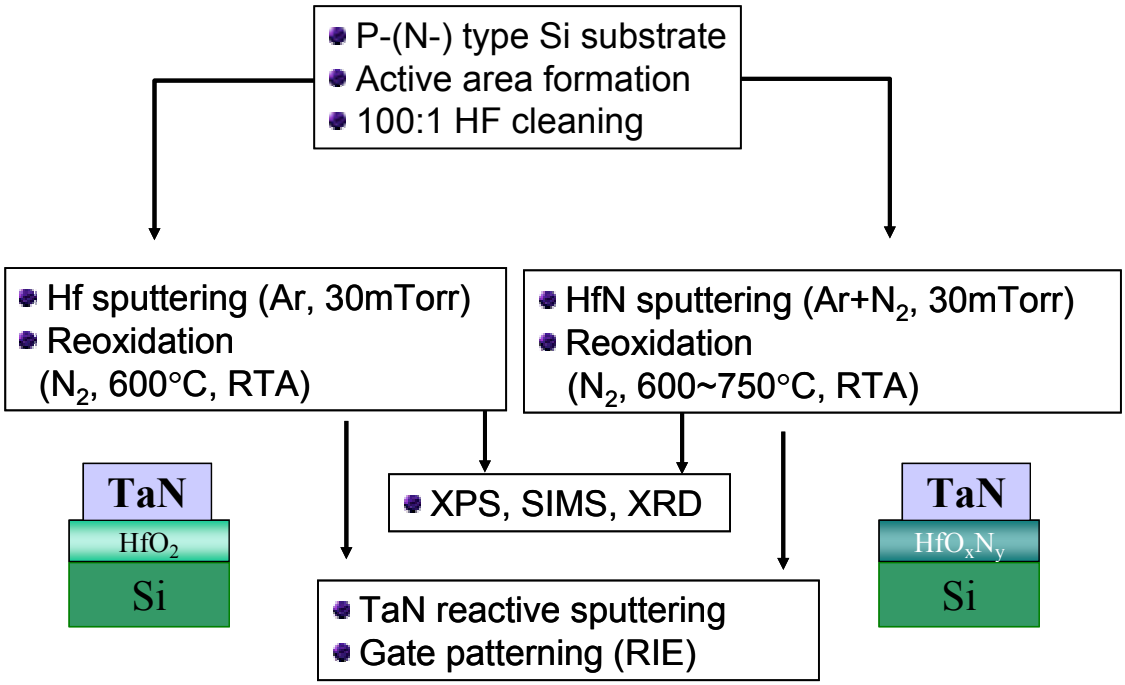

Figure 5.1.1 MOSFET fabrication process for HfON and HfO_2 (Continued).

- Source/Drain implantation
  (BF_2 50keV, $5x10^{15}/cm^2$, or P 50keV, $5x10^{15}/cm^2$)
- Low temperature CVD oxide (~150 nm) deposition
- Source/Drain activation (~950°C, 30 sec.)
- Contact patterning
- Al (~500 nm) sputtering and patterning (wet etching)
- Al deposition on wafer back side
- Forming gas anneal (450°C, 30 min)

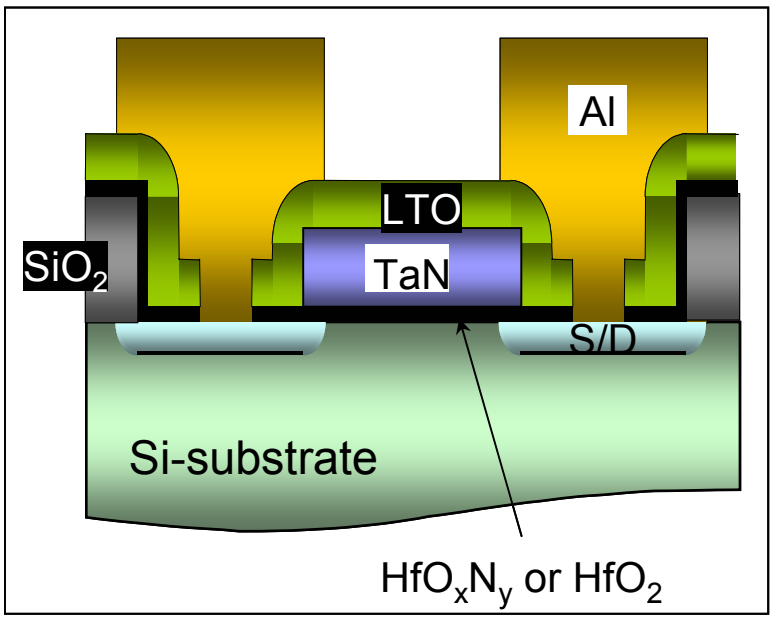

Figure 5.1.2 MOSFET fabrication process for HfON and HfO_2 (after gate patterning) and the final MOSFET structure.

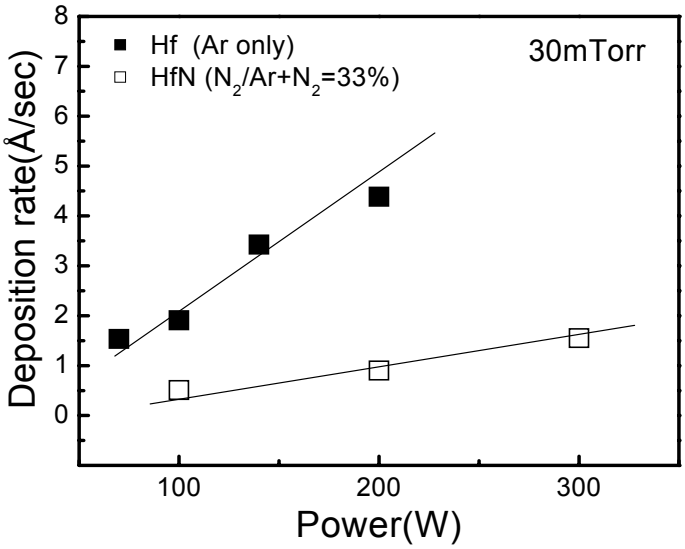

Figure 5.2 Deposition rate of Hf and HfN on Si substrate as a function of discharging power at 30mTorr.

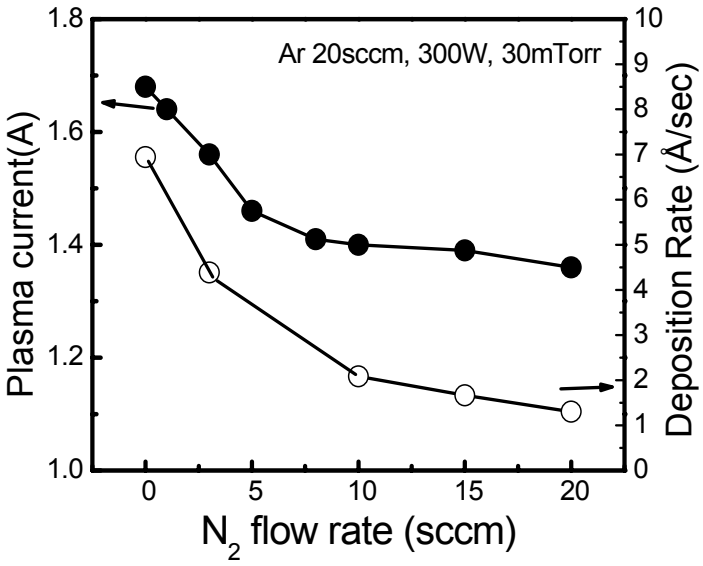

Figure 5.3 Plasma current vs. nitrogen flow rate (Ar=20sccm, 300W, 30mTorr)

PDA temperature dependence of EOT and leakage current was investigated with temperatures from 600ºC to 750ºC (time = 1 min.). To avoid excessive oxidation which would result in the formation of a thick interfacial layer between Si and high-*k* dielectrics, PDA was performed in a N_2 ambient. The residual oxygen in the annealing chamber and the oxygen absorbed in the HfN film were sufficient to oxidize the HfN films and convert it into Hf-oxynitride (for PDA temperatures ≥650ºC). To compare thermal stability in terms of EOT increase due to post metal-gate (PMA) temperature, PMA temperature was varied from 600ºC to 950ºC.

TaN electrode was deposited by dc reactive sputtering in a Ar+N_2 ambient with 10 mTorr of chamber pressure and 6.0 W/cm^2 of plasma power density. Sheet resistance of the TaN film was approximately 10 Ω/square. The TaN gate was patterned by reactive ion etch using a CF_4/Cl_2 mixture as the etching gas. Before measurements of capacitor characteristics, Al was deposited on the backside of the samples to ensure lower contact resistance. Capacitance curves and leakage current were measured by a HP 4194 LCR meter and a HP 4156 semiconductor parameter analyzer, respectively. EOT was extracted from the C-V curve measured at 1 MHz after considering the quantum mechanical effect. The area of the capacitor was $5x10^{-5}$cm^2.

A PDA in a N_2 ambient was found to be more effective to avoid excessive oxidation than an O_2 PDA which would result in a formation of thick interfacial layer between the Si substrate and the high-*k* dielectrics. Fig.5.4 shows increases in physical thickness of HfO_2 and HfON as a function of the ambient (O_2 and N_2) and temperature of the PDA. HfN films suppress increase of physical thickness arising from oxygen diffusion during the PDA. The suppressed increase in the physical thickness during PDA was observed in the HfON film. This fact can be explained in a similar way to Si-N bond in silicon oxynitride film in which incorporated nitrogen reduced increase of

physical thickness of dielectric layer during the reoxidation of silicon oxynitride film [29]. PDA temperatures higher than 700ºC are found to be inappropriate for devices requiring EOT < 10 Å because of the unacceptably increased EOT during PDA.

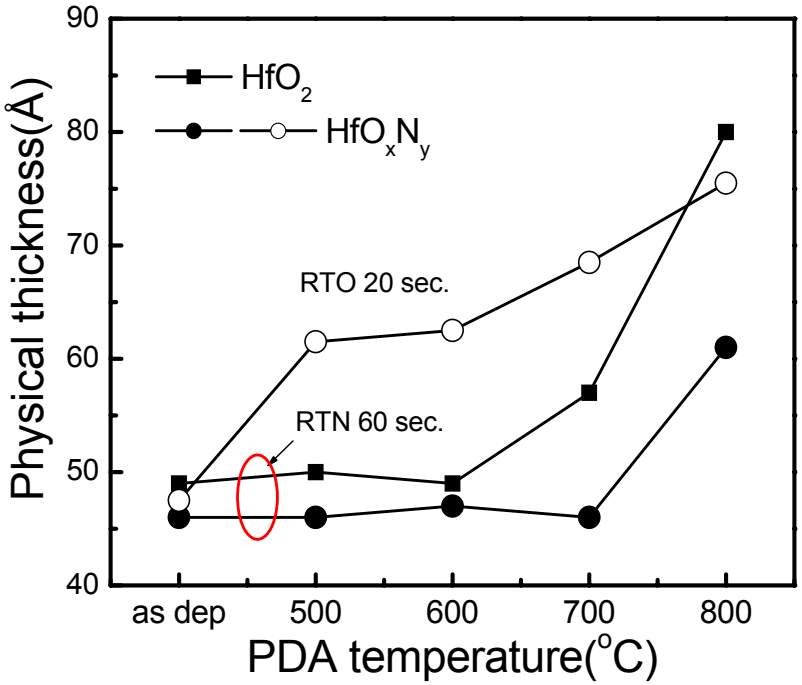

Figure 5.4 Physical thickness variation as a function of PDA temperature and ambient.

Figure 5.5 shows variations of EOT and leakage current density (J) measured at -1.5 V of TaN/HfON(~50Å)/p-type Si as a function of PDA temperature ranging from 600ºC to 750ºC. At 600ºC, large J (>0.1 mA/cm^2) was obtained, presumably due to insufficient oxidation of the HfN film. With PDA temperature above 650ºC, leakage current was reduced to less than 1 mA/cm^2. However, EOT increases rapidly at 650ºC and above. Considering the trade-off between EOT and leakage current, 650ºC was chosen as an optimized PDA temperature.

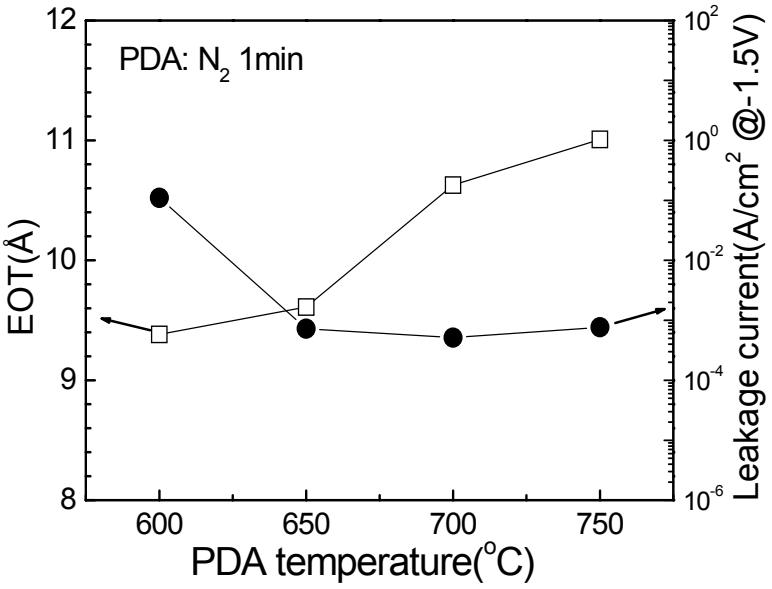

Figure 5.5 EOT and J variation as a function of PDA temperature in N_2 ambient.

5.2 MATERIAL ANALYSIS OF HFON FILM

5.2.1 Bonding status of HfON film

Using X-ray photoelectron spectroscopy (XPS) analysis, chemical bonding states of four gate dielectrics (~50Å) were compared: (a) HfO_2 without PDA, (b) HfO_2 with PDA, (c) HfO_xN_y without PDA, and (d) HfO_xN_y with PDA. Conditions for HfO_2 deposition were detailed in chapter 4. XPS were analyzed *ex situ* and all peaks were referenced to Si_{2p} at 99.3 eV.

Figure 5.6 (i) shows XPS spectra for the Hf_{4f} regions for samples (a), (b), (c), and (d). Except for sample (c) [i.e. HfON without PDA], Hf_{4f} peaks for the other three samples show a sharp doublet according to spin-orbit splitting into the $Hf_{4f5/2}$ and $Hf_{4f7/2}$. For sample (c), broad triple peaks which can be assigned to Hf-O and H-N bonds were observed. Hf-N bond in this sample is located at 15.8 eV, which is shifted 0.5 eV from the Hf-N binding energy (15.3 eV) reported for $HfN_{0.19}$ [30].

Similarly, the Hf-O peak is also shifted from ideal binding energy by 0.4 eV. The shift of binding energy of the Hf-N bond to a higher binding energy as well as the shift of the Hf-O bonding energy to a lower binding energy from their reported positions indicate the presence of Hf-O bonds in addition to Hf-N bonds in the nitrogen-incorporated films. For the HfO_2 samples (a) and (b) [HfO_2 with and without PDA, respectively], the binding energies corresponding to $Hf_{4f5/2}$ and $Hf_{4f7/2}$ were located at 19.5 eV and 17.8 eV, respectively, which agree well with the reported values of 19.64 eV and 17.93eV for $Hf_{4f5/2}$ and $Hf_{4f7/2}$ peaks for HfO_2 [31]. Negligible difference between (a) and (b) was observed. On the other hand, XPS peaks of sample (c) were converted to doublet peak-type after PDA. This indicates that Hf-N bonds were replaced by Hf-O bonds after the

PDA at 650ºC. However, each Hf_{4f} peak of sample (d) showed a noticeable shift (~0.25 eV) from ideal HfO_2 peaks, which implies the presence of remaining Hf-N bonds in the films.

Figure 5.6 (ii) shows N_{1s} peaks for the four samples. Sample (a) and (b) show no peaks for N_{1s}, while sample (c) and (d) show noticeable N_{1s} peaks. N_{1s} peak of (d) (397.8eV) corresponds to Si-O-N bonds (~398 eV [32]), while 396 eV of (c) can be attributed to Hf-N bonds. The presence of Si-O-N peaks in sample (d) is similar to the HfO_2 films deposited on NH_3 nitrided Si surface [13].

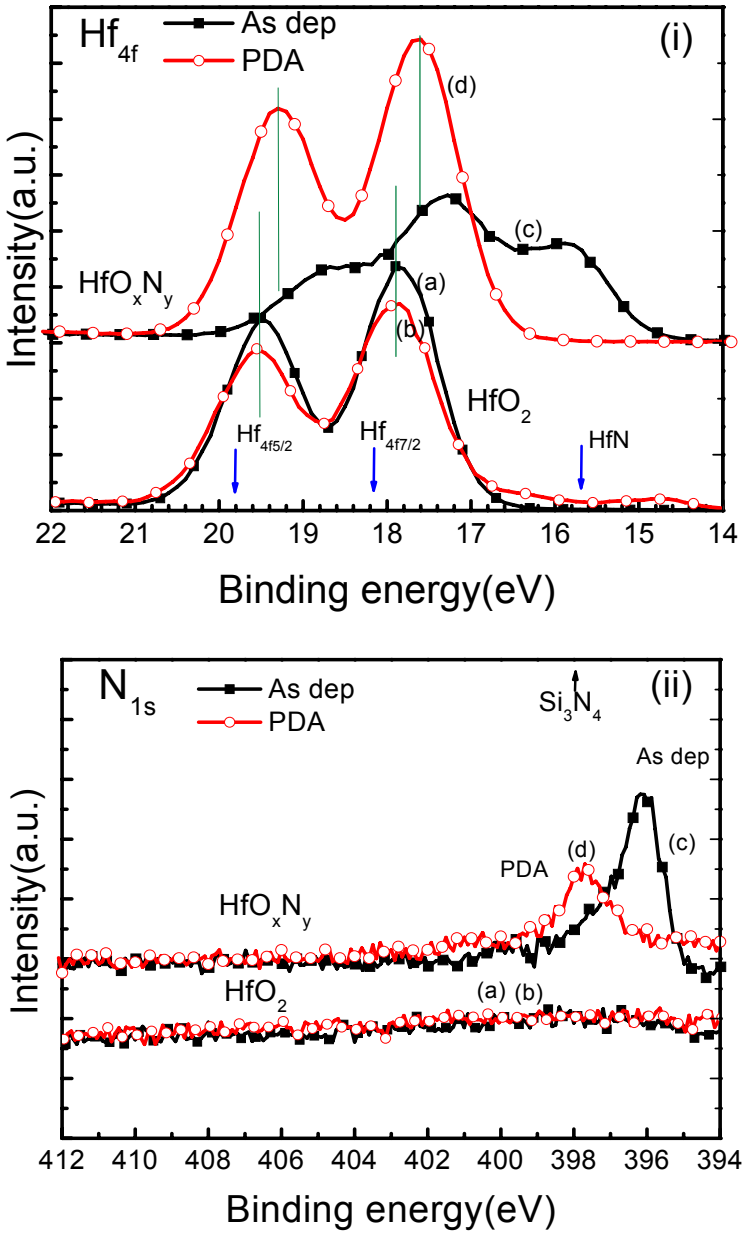

Figure 5.6 XPS spectra for Hf_{4f} (i) and N_{1s} (ii) region for four 50 Å-thick dielectrics deposited on p-Si substrate: (a) HfO_2 without PDA (b) HfO_2 with PDA (c) HfON without PDA (d) HfON with PDA. PDA was performed at 650ºC, for 1 min, in a N_2 ambient using atmosphere rapid thermal anneal (RTA).

5.2.2 Nitrogen profile of HfON film

Depth-profile and amount of incorporated nitrogen as well as chemical bonding states are major factors which affect material and electrical characteristics of the HfON dielectrics. Figure 5.7 (a) and (b) exhibit TOF SIMS depth profiles of chemical species in the 50Å-thick HfO_2 and HfON deposited on Si substrates after PDA at 650℃ for 1 min under nitrogen ambient, respectively. In the both films, the presence of interfacial layer (IL) between dielectric and Si substrate can be obviously inferred from the silicon profiles in which there exists an intermediate layer with a ~45% count of the Si substrate. It is to be pointed out that the physical thickness of IL may not be exactly extracted from the sputtering time because sputtering yield of chemical species depends on the dielectrics. Both films showed almost identical oxygen profiles which indicate that HfN was completely converted to HfON.

In the SIMS measurement, nitrogen was not able to be detected in the form of element but chemical species such as SiN and HfON. HfON film showed approximately 20 times larger count of SiN than HfO_2 film which appears to have a noise level of SiN. Note that SiN exists mostly at the IL between Si substrate and dielectrics in the HfON film. The enhanced nitrogen amounts at the dielectric/substrate interface in the HfON films can be attributed to the interfacial strain between the dielectric and Si in a similar way as in silicon oxynitride (SiON) film on Si substrate [19]. In the HfON film, nitrogen was detected also in the form of HfON in the bulk of the dielectrics. The IL composition of the HfON films appears to be hafnium-silicon-oxynitride (HfSiON-like) from the SIMS results which exhibit presence of chemical species including Hf, Si, O and N at the interface. In contrast, the IL of the HfO_2 films seems to be hafnium-silicate (HfSiO) from the SIMS profile.

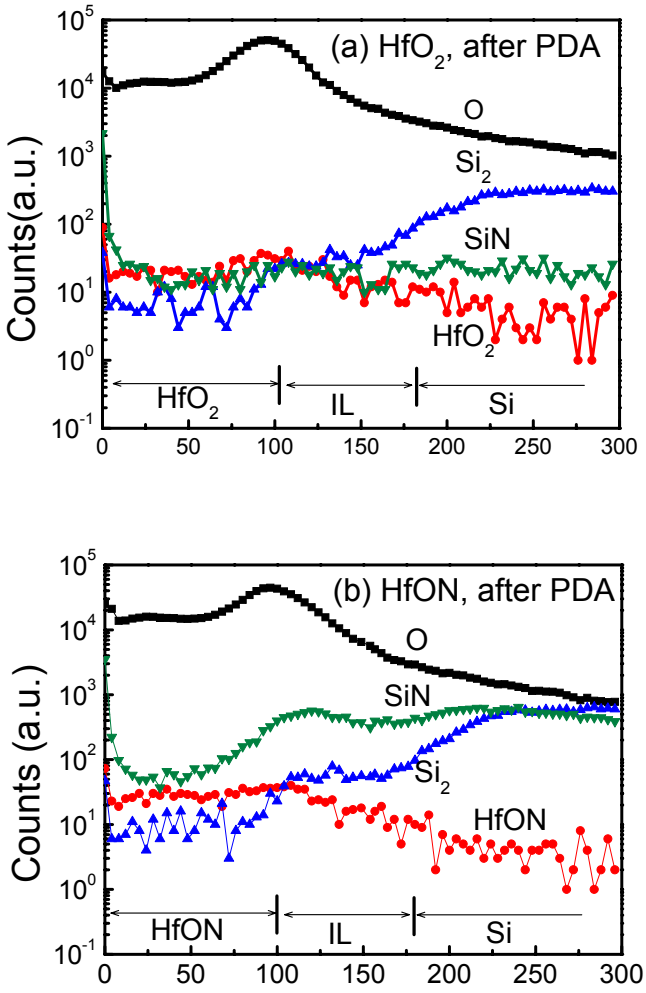

Figure 5.7 TOF SIMS depth profiles of chemical species in 50Å-thick HfO_2 (a) and HfON (b) films deposited on Si substrates. For both films, interfacial layers existed between dielectric and Si substrates. In HfON, nitrogen detected in the form of SiN piled up at the interfacial layer.

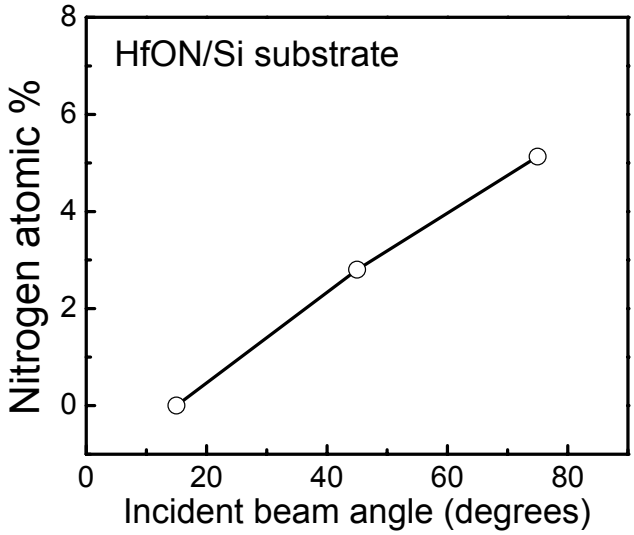

Figure 5.8 Nitrogen atomic % of 50-Å-thick HfON deposited on a Si substrate as a function of incident beam angles in XPS analysis. The larger angle reflects information from the closer layer to Si substrates.

Angle-resolved XPS was used to investigate atomic composition of the incorporated nitrogen in the HfON film and compare the chemical bonding states of HfO_2 and HfON films. Figure 5.8 shows nitrogen atomic % of HfON film as a function of incident beam angles (15^o, 45^o, and 75^o). The higher incident beam angle reflects information from the deeper layer (i.e. the closer layer to the dielectric/the Si substrate interface) of the film. Nitrogen atomic compositions of ~0, 2.8, and 5.2% were observed for incident beam angles of 15^o, 45^o, and 75^o, respectively. The nitrogen composition measured by angle-resolved agrees well with the results of SIMS profiles which indicates that nitrogen piles up at the dielectric/Si interface.

5.2.3 Crystallization of HfO_2 and HfON films

The silicon dioxide that has been used as the gate dielectric for more than the past 30 years remains in amorphous state after all integration device process. In addition to the excellent interface quality of the SiO_2, the amorphous phase provided a film uniformity (in terms of thickness, impurity penetration, roughness, and consequently electrical properties), which would not be achieved in poly-crystalline phase [33].

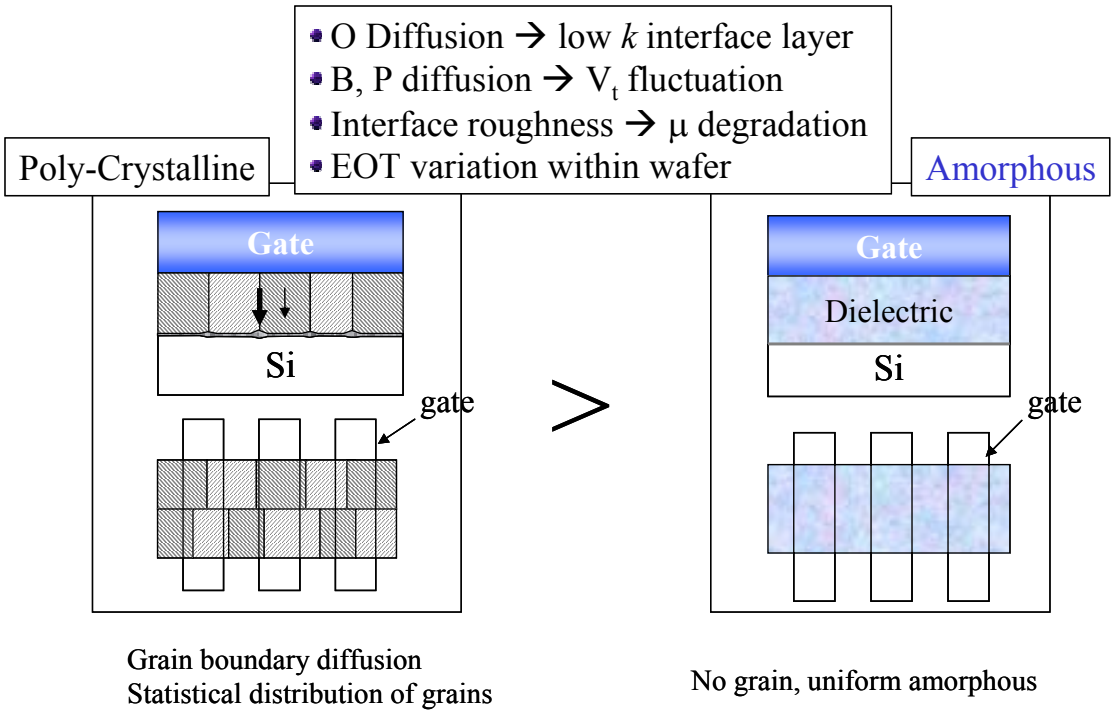

Figure 5.9 Comparison of integration concerns between poly-crystalline and amorphous dielectrics.

Figure 5.9 summarizes advantages of amorphous phase over crystalline phase as gate dielectrics. In general, atomic diffusion along grain boundaries is faster than through the bulk of the grains. This assumes that atoms have lower activation energy of motion in the boundary layer and that vacancy formation is easier because of the excess volume in the boundary [34]. Therefore, oxygen diffuses more easily through the poly-crystalline films than through the amorphous film. Faster oxygen diffusion will induce a growth of thicker low-k interfacial layer for the poly-crystalline dielectrics. More deleteriously, low-k interfacial layer of poly-crystalline dielectric would be rougher due to the difference in the bulk diffusion constant (D_b) and grain boundary diffusion constant (D_g). This enhanced roughness consequently will degrade the channel mobility of MOSFETs at higher effective electric field (E_{eff}).

In particular, poly-crystalline gate dielectric collaborated with poly-Si gate technology will suffer an enhanced V_{th} fluctuation arising from the fast diffusion of dopants through the grain boundaries. Another disadvantage of the poly-crystalline dielectrics is imposed on the device-to-device non-uniformity of EOTs stemming from statistical distribution of crystalline grains: Each grain may have different degree of crystallization and the average EOT of transistors may vary depending on the crystallinity of the gate dielectrics. Although leakage current increase of HfO_2 arising from crystallization has been reported to be negligible in contrast with Ta_2O_5, mechanical stress due to phase transformation induces weak bonds or defects in the dielectric or at the dielectric/Si interface.

Most high-k dielectrics except Al_2O_3 remains poly-crystalline after subsequent anneal process [33]. Unfortunately, dielectric constant of Al_2O_3 (~9) appears to be too low to sustain more than two generation of MOSFET devices below 100nm node and below. To retard the crystallization of high-k dielectrics, several methods have recently

been proposed: i) introduction of silicates such as hafnium silicate and zirconium silicate ii) multi-cation oxides such as (Hf,Al)O_2 and (Zr, Al) O_2 by adding dopants into HfO_2 or ZrO_2, and iii) metal oxynitrided such as HfON [35] and ZrO_xN_y [27]. Although Al is known to retard crystallization of HfO_2, the dielectric constant is degraded as the Al content increases [26].

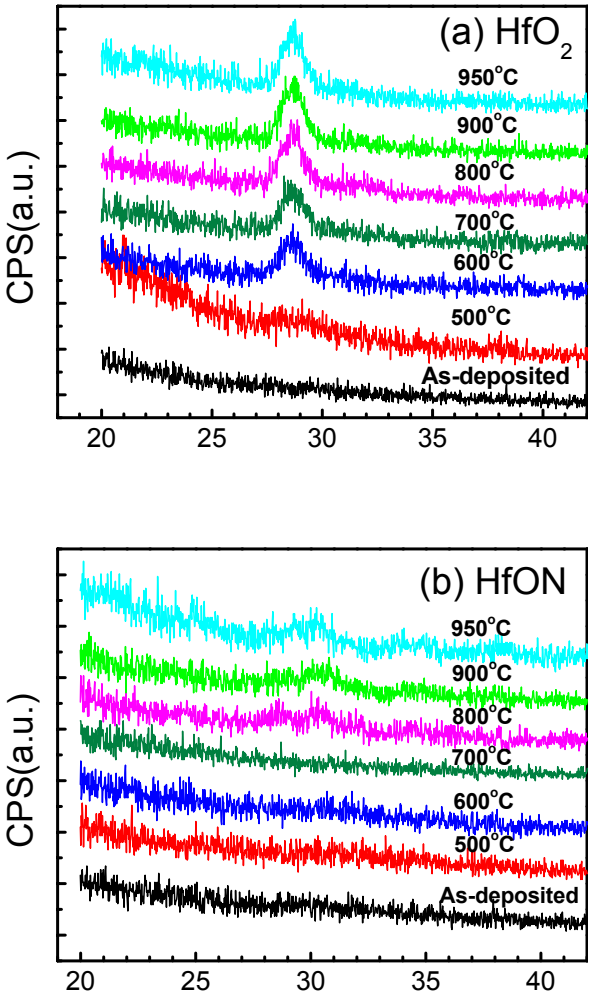

Figure 5.10 XRD patterns of ~ 100Å-thick-HfO_2 and HfON as a function of PMA temperature on the Si (100) wafers.

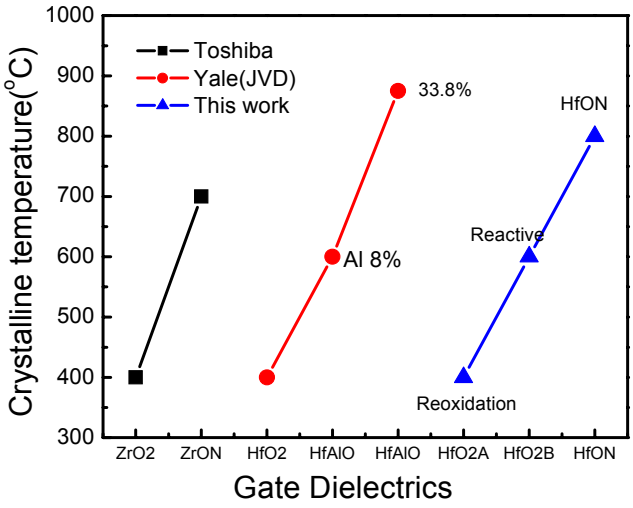

Figure 5.11 Comparison of crystallization temperature of various high-k dielectrics.

Glancing-angle (alpha = 3º) XRD was used to investigate crystallization behavior of HfO_2 and HfON film. To ensure sufficient XRD counts, thicker films for XRD analysis were used that for electrical characterization. Figure 5.10 compares crystallization behaviors for HfO_2 sputtered by reactive sputtering and HfON. HfON film (100Å) starts to crystallize at ~800ºC while HfO_2 (100Å) films at 600ºC. The crystallization temperature of HfON is ~200ºC higher than those of HfO_2 and ZrO_xN_y (Fig.11). Nitrogen incorporation into HfON film suppresses the crystallization of dielectric films without any degradation of dielectric constant. By optimization of the contents of incorporated nitrogen and process conditions, further increase in the crystallization of the HfON is required to remain in "amorphous phase" of HfON after annealing process expected in the advanced MOSFET process.

The crystallinity of the HfON film after 950℃ anneal was further investigated using high-resolution TEM. Figure 5.12 shows a planar TEM picture of the film with an inset of a selected area diffraction (SAD) pattern. The planar image and the ring pattern of the SAD reveal that the grains of the film are randomly oriented with grain sizes of a few-tens nanometer in diameter.

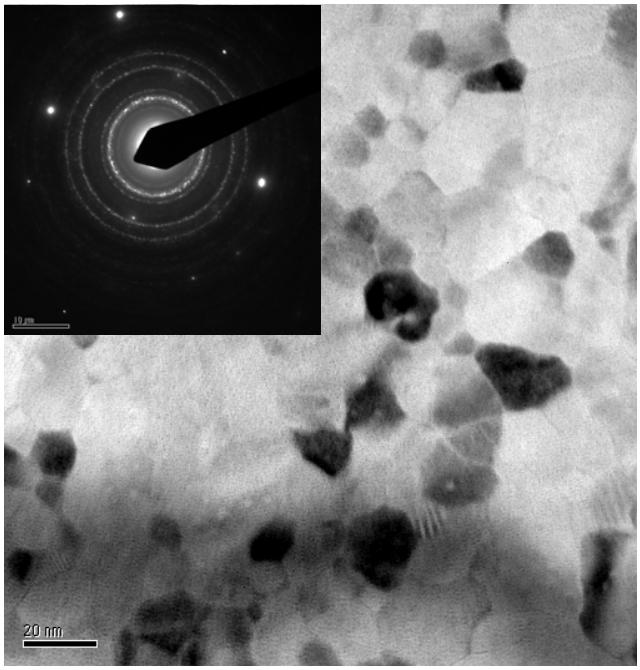

Figure 5.12 Planar TEM picture of 100Å-thick HfON with an inset of a selected area diffraction (SAD) pattern.

5.3 SUMMARY

Electrical and material characteristics of hafnium oxynitride (HfON) gate dielectrics have been studied in comparison with HfO_2. HfON was prepared by a deposition of HfN followed by post-deposition-anneal (PDA). By secondary ion mass spectroscopy (SIMS), incorporated nitrogen in the HfON was found to pile up at the dielectric/Si interface layer. Based on the SIMS profile, the interfacial layer (IL) composition of the HfON films appeared to be like hafnium-silicon-oxynitride (HfSiON) while the IL of the HfO_2 films seemed to be hafnium-silicate (HfSiO). HfON showed an increase of 300℃ in crystallization temperature compared to HfO_2.

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Chapter 6: Electrical Properties of HfON gate dielectrics: MOS capacitor and transistors

6.1 ELECTRICAL CHARACTERIZATION OF MOS CAPACITORS

6.1.1 C-V and JV characterization

Figure 6.1 (a) and (b) shows typical CV and JV curves of MOS capacitors with HfO_2 and HfON dielectrics. The physical thicknesses measured by ellipsometry were 47Å and 52Å for HfO_2 and HfON films, respectively. In Fig 6.1 (a), the HfON capacitor exhibited lower flat band voltage (V_{fb}=-0.50V) than HfO_2 (-0.25V). The lowered V_{fb} in the HfON indicates that the addition of nitrogen involves positive fixed charges (Q_f) similarly to silicon oxynitrides [1]. In Fig 6.1 (a), the corresponding EOT of HfON capacitor was 8.8Å which is 3Å thinner than that of HfO_2 capacitors with an EOT of 11.8Å. Leakage currents of the two capacitors are compared in Fig.6.1 (b). Leakage currents at -1.5V were 5 mA/cm^2 and 1.5 mA/cm^2 for HfO_2 and HfON, respectively. Notice that HfON with a thinner EOT showed a lower leakage current than HfO_2.

Figure 6.2 shows leakage currents of HfON compared to HfO_2 for various EOTs ranging from ~7.6 Å to ~ 20 Å. To exclude the effect of flat-band voltage difference between two groups, leakage currents measured at $|V_g-V_{fb}|$=1V were plotted against EOTs in Fig.6.2. All the data in Fig.6.2 were collected for TaN/HfO_2(or HfON)/p-type Si MOS capacitors before and after PMA. HfON shows an advantage in terms of J vs EOT over HfO_2 after PMA rather than before PMA; HfON dielectrics exhibit ~10x lower J than HfO_2 for the same EOTs before PMA, while ~40x lower J after PMA. The better thermal stability of HfON implies that HfON dielectric might be more suitable for gate dielectric application with self-aligned gate process. The lower leakage current of HfON

can be attributed to its thicker physical thickness to achieve a given EOT due to the higher dielectric constants of bulk and interface layer compared to HfO_2, as discussed in the following paragraphs. Since leakage current of the thin dielectric (~50Å) are governed by tunneling mechanism [2], an increased physical thickness can result in a drastic decrease in leakage current.

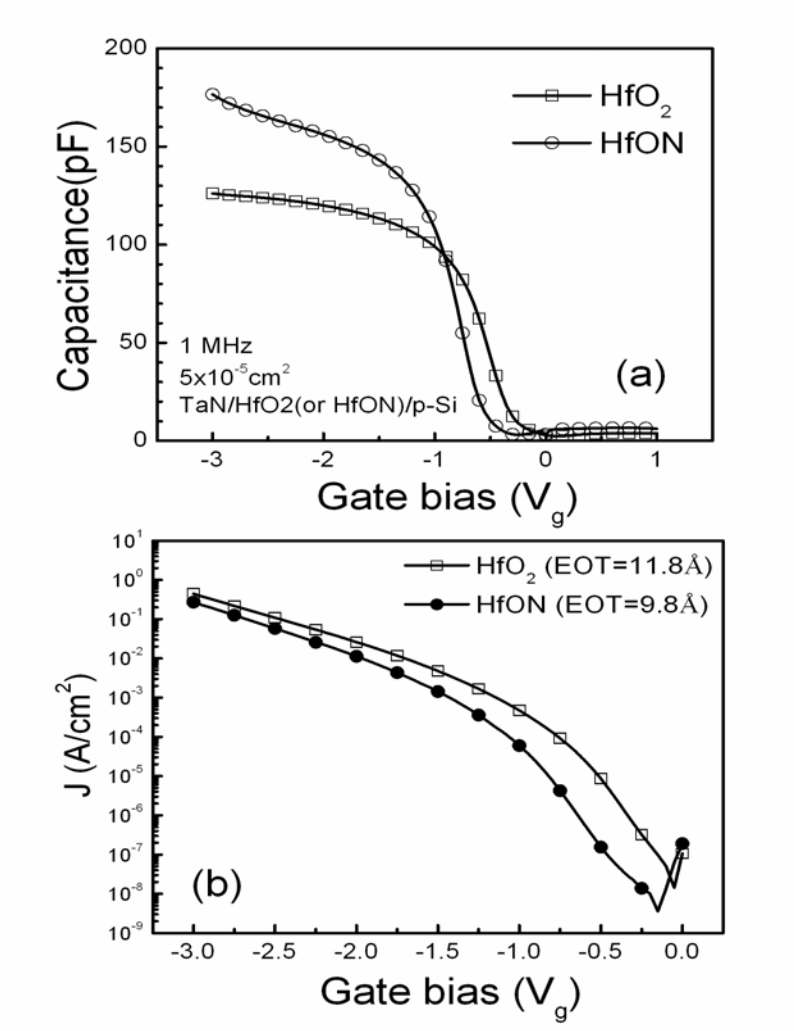

Figure 6.1 Typical CV (a) and JV (b) curves of MOS capacitors with HfO_2 and HfON dielectrics. The physical thicknesses measured by ellipsometry were 47Å and 52Å for HfO_2 and HfON films, respectively.

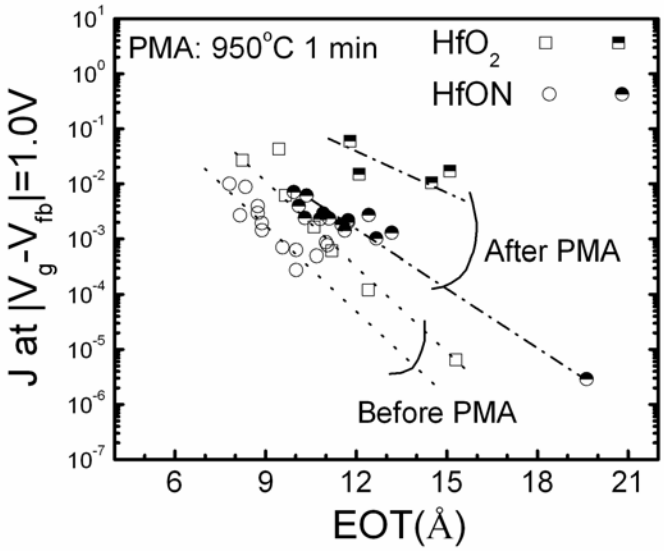

Figure 6.2 Leakage currents (J) of HfON compared to HfO_2 for various EOTs ranging from ~7.6 Å to ~ 20 Å. To exclude the effect of flat band (V_{fb}) difference between two groups, leakage currents measured at $|V_g-V_{fb}|$=1V were plotted against EOTs.

6.1.2 Thermal stability of MOS capacitor

EOT increases during high-temperature PMA by interfacial layer growth due to the oxygen diffusion through the gate electrode or excessive oxygen in the dielectrics [3]. This may inhibit the use of high temperature processing after gate electrode fabrication such as source and drain activation. For various dielectric groups (i.e., HfO_2, HfO_2 on the surface-nitrided Si, HfO_2 with top nitridation and HfON) with the physical thickness of ~50-Å, EOT variations were plotted as a function of PMA temperature in Fig.6.3. PMA was performed for 1 min in a N_2 ambient. After PMA at 950 ºC, EOT increased from 10.6 Å to 14.2 Å for HfO_2, whereas the EOT increase was suppressed to less than 0.5 Å in the HfON. Even after PMA at 950ºC, low EOT (10.4 Å) was

obtained while keeping leakage current less than 1 mA/cm^2 using HfON. The superior thermal stability of HfON can be explained by the role of Si-N bonds at the dielectric/Si substrate, which was proposed to suppress oxygen diffusion in the study of NH_3 surface nitridation [3, 4]. The increase of EOT in HfON is less than that in surface nitridation (~1.5Å) [3]. This fact indicates that the nitrogen bonding in the bulk-HfON as well as the nitrogen bonds at the dielectric/Si substrate inhibits oxygen diffusion through the gate dielectric, eventually resulting in the suppression of low-k interfacial layer formation.

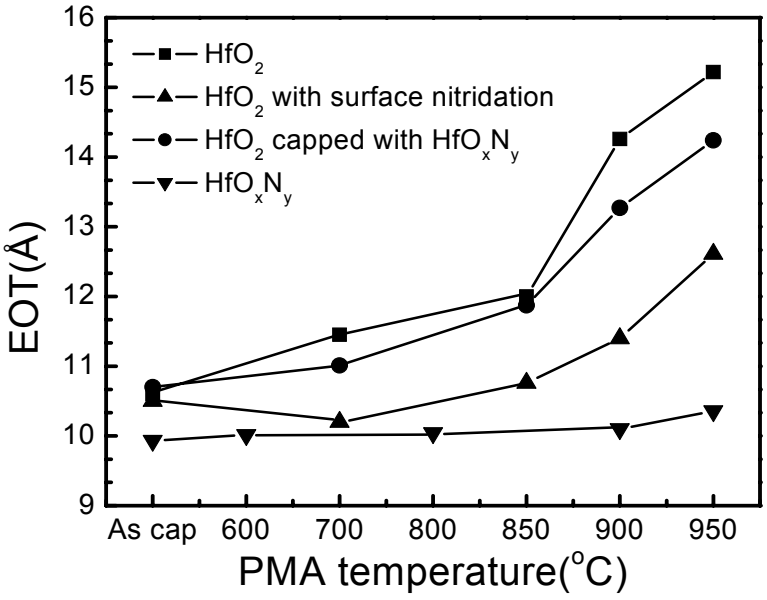

Figure 6.3 EOT variations as a function of PMA temperature under N_2 ambient for 1 minute. EOT increase was suppressed < 1 Å in the HfON MOS capacitor.

6.1.3 Dielectric constant of HfON films

Figure 6.4 shows EOTs as a function of dielectric thickness measured by ellipsometry for HfO_2 and HfON. The dielectric constant (k) of the bulk film can be obtained from the slope of the EOT plot against dielectric thickness (t). The extracted bulk dielectric constants for HfO_2 and HfON were 19 and 22, respectively. The HfON showed an increase of ~ 16% in the bulk dielectric constant compared to HfO_2. The increase of dielectric constant in the HfON might be attributed to the enhancement of electron polarization and ionic polarization by incorporated nitrogen atom in a similar way reported in HfSiON [5].

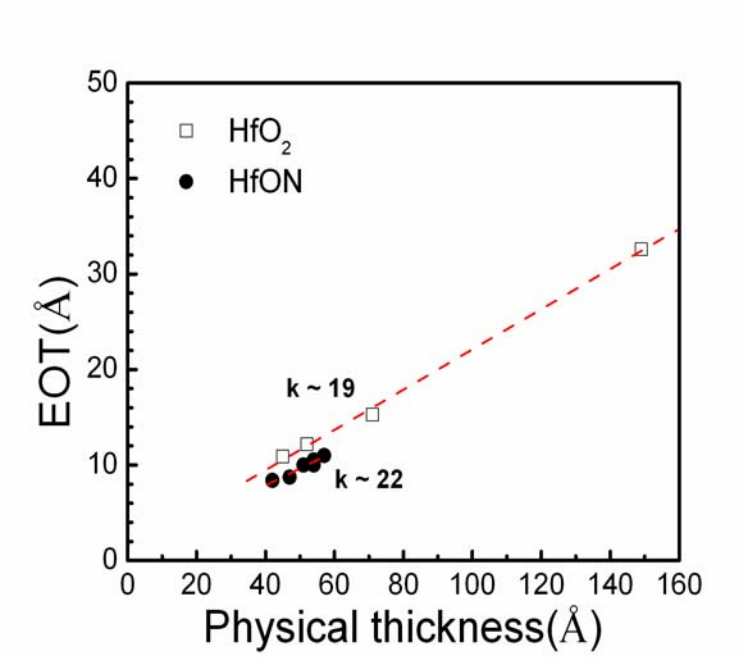

Figure 6.4. EOTs as a function of dielectric thickness measured by ellipsometry for HfO_2 and HfON. A bulk dielectric constant (k) of the film is proportional to 1/slope of the EOT plot against dielectric thickness (t).

To investigate dielectric constant of ILs, high-resolution TEM pictures of HfON and HfO_2 were analyzed. Figure 6.5 shows TEM pictures for HfO_2 (EOT=14Å) and HfON (EOT = 11Å) after post-metal-anneal (PMA) at 950℃ for 1 min in nitrogen ambient. The PMA condition has a thermal budget sufficient for the activation of source and drain in the self-aligned process. Note that the physically thicker HfON showed a lower EOT than HfO_2. As shown in Fig. 6.5, both dielectrics have ILs with a similar thickness of 15 Å whereas bulk-HfON (40 Å) is thicker than bulk-HfO_2 (34 Å). Using the bulk dielectric constants (k_{bulk}) measured in Fig. 8, the IL dielectric constant (k_{IL}) can be calculated using equation (6.1),

$$EOT = \varepsilon_{SiO_2}\left(\frac{t_{IL}}{k_{IL}} + \frac{t_{bulk}}{k_{bulk}}\right) \quad (6.1),$$

where interface later thickness (t_{IL}) and bulk thickness (t_{bulk}) can be obtained from the TEM pictures. The calculated dielectric constant of interfacial layer in HfON was ~14, which is larger than that of HfO_2 (~7.8). As discussed in the SIMS profiles, the IL of HfON was HfSiON-like, and that of HfO_2 was similar to HfSiO. According to a report on the HfSiON [5], dielectric constant of HfSiON increases with the addition of nitrogen. Thus, the presence of nitrogen at the IL of the HfON accounts for the increase in the dielectric constant of the film. This fact indicates that nitrogen incorporated hafnium silicate (HfSiON) shows higher dielectric constant than hafnium silicate (HfSiO) for the same amount of Hf/Si ratio.

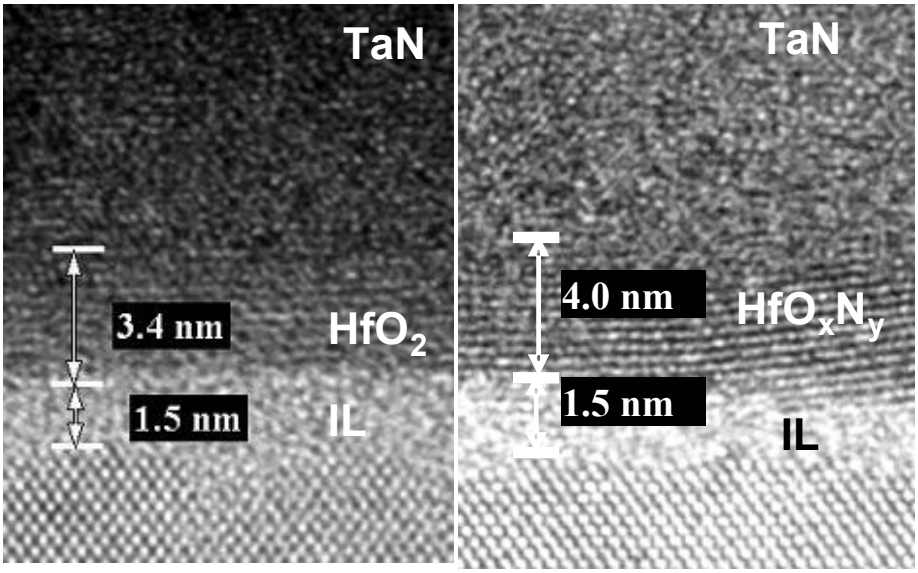

Figure 6.5 High-resolution TEM pictures of HfO_2 (EOT=14Å) and HfON (EOT = 11Å) after post-metal-anneal (PMA) at 950℃ for 1 min under nitrogen ambient. Physically thicker HfON showed a lower EOT than HfO_2.

6.1.4 Hysteresis and TZDB

CV hysteresis of high-k gate dielectrics has been known as one of potential problems which may limit the application because the hysteresis leads to instability of threshold voltage of MOSFETs. In Fig. 6.6, hystereses of HfO_2 and HfON were compared for before and after PMA. The hysteresis was defined as a difference between flat band voltages of CV curves swept from -2V to 1V and vice versa. As shown in Fig.10, HfON shows higher hysteresis than HfO_2 for both before and after PMA, and PMA reduces hysteresis for both capacitors. HfON shows hystereses of 350 mV and 50 mV for before and after PMA, respectively whereas HfO_2 shows 30 mV and 8 mV for each condition. This result indicates that parts of trapped charge were relieved by the annealing. Typical CV hystereses of HfON are shown in the inset of Fig.6.6. Note that flat band voltages increased after PMA in addition to the decrease of hysteresis.

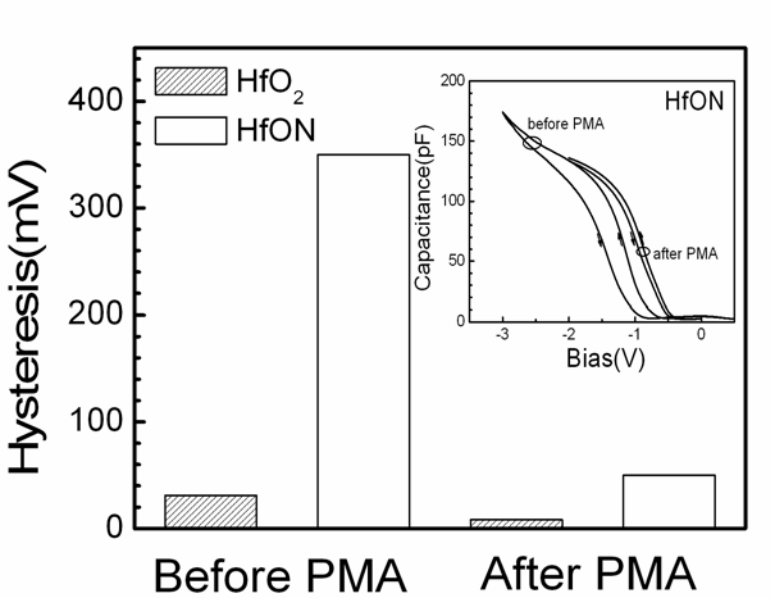

Figure 6.6 Comparison of hystereses of HfO_2 and HfON for before and after PMA. Typical CV hystereses of HfON are shown in the inset.

Ramped voltage test (i.e., Time Zero Dielectric Breakdown) was performed to compare dielectric strength of HfO_2 and HfON. Figure 6.7 shows TZDB characteristics measured for nMOS capacitors before and after PMA. Irrespective of the PMA, the HfON showed higher an improved effective breakdown field (E_{bd}) than HfO_2 when

$$E_{bd} = \left| V_{bd} - V_{fb} \right| / EOT \qquad (6.2),$$

where V_{bd} represents the breakdown voltage, and flat band voltage (V_{fb}) was subtracted from it to compensate for the slight difference in V_{fb} between HfO_2 and HfON. By equation (6.3), much higher electric field is applied to the ILs since they have lower dielectric constants than the bulk layers as discussed before,

$$\varepsilon_{IL} E_{IL} = \varepsilon_{bulk} E_{bulk} \qquad (6.3),$$

where E_{IL} and E_{bulk} represent electric fields of the interface layers and bulk layers of the dielectrics. Thus, dielectric breakdown is believed to be dominated by the breakdown in the ILs. Therefore, the improved breakdown field in the HfON can be explained by the difference in ILs between the two groups rather than bulk layers.

The PMA affects TZDB characteristics differently for both groups; by PMA, E_{bd} was improved for HfON whereas it was degraded for HfO_2. Along with the advantages of HfON in terms of J vs. EOT after PMA, this result indicates that HfON is more suitable for the application into the self-aligned gate process. Considering similar effects of nitrogen on the ZrON [6], and SiON [7], the role of nitrogen in the dielectric breakdown seems to be similar for metal-oxide-based dielectrics.

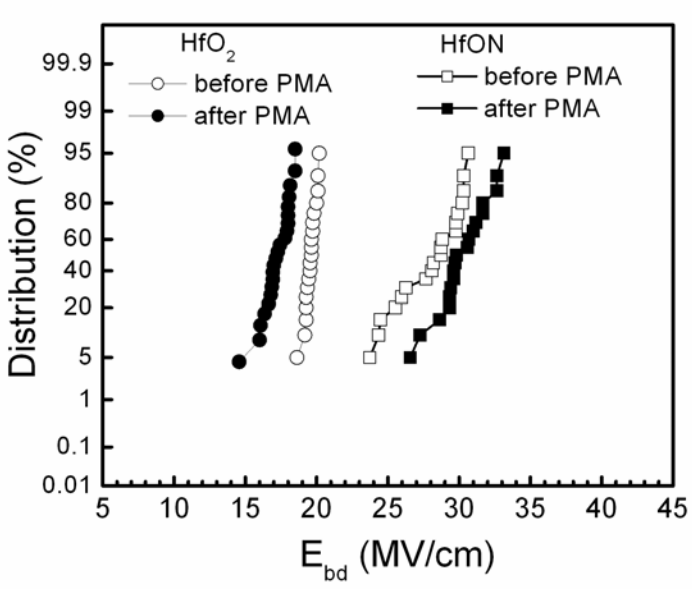

Figure 6.7 TZDB characteristics measured for nMOS capacitors before and after PMA. Effective breakdown field (E_{bd}) were defined as $E_{bd} = \left|V_{bd} - V_{fb}\right| / EOT$.

6.2 ELECTRICAL CHARACTERIZATION OF MOS CAPACITORS

6.2.1 Typical transistor characteristics

Using the HfON as gate dielectric, well-behaved I_d-V_g (Fig.6.8) and I_d-V_d (Fig. 2.15) characteristics were obtained for both p and nMOSFET with TaN gates (W/L = 150 μm / 10 μm). Subthreshold swings of 73 mV/dec and 80 mV/dec were obtained for p and nMOSFET, respectively. PMOSFET showed significantly low off-state current (I_{off} ~ 30fA/μm), while nMOSFET showed slightly higher I_{off} (~30 pA/μm). Threshold voltage (V_{th}) for nMOSFET was 0.4V while –0.7V for pMOSFET. The drive current (I_{dsat} @V_g-V_{th} = +/-2 V) was 42 mA/μm and 8.3mA/μm as shown in Fig. 6.9, respectively.

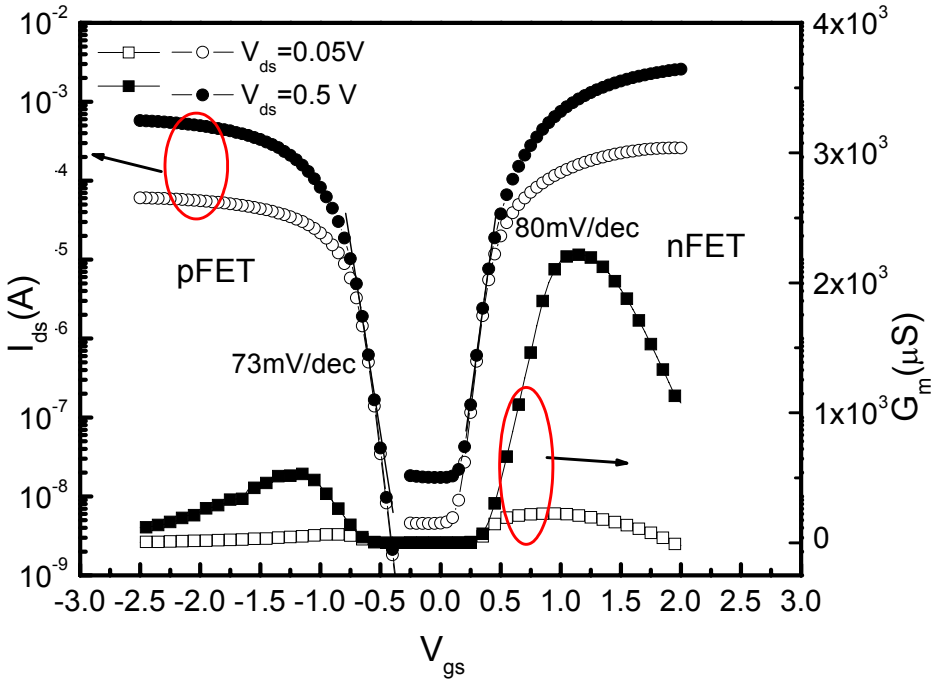

Figure 6.8 Ids-Vgs curves for nMOSFET and pMOSFET with 50Å-thick HfON gate dielectrics (W/L=150μm/10μm).

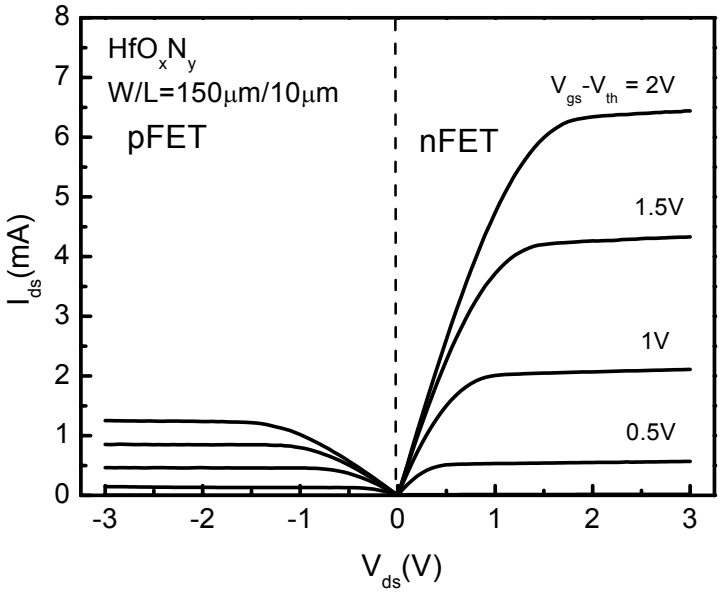

Figure 6.9 Ids-Vds curves for nMOSFET and pMOSFET with 50Å-thick HfON gate dielectrics (W/L=150μm/10μm).

6.2.2 Effects of high-temperature forming gas anneal on MOSFET performance

Transistor characteristics of HfON gate dielectrics (EOT~13.2Å) were investigated using nFETs with a dimension of gate width/length (150μm/10μm). As expected from the flat-band shift due to fixed charge and hysteresis, the charges in the HfON may degrade device performance. High temperature FG anneal (FTFG) has been reported to improve transistor performance of MOSFETs with poly-Si gated HfO_2 [8], TaN-gated HfO_2 [9], and ZrON [6]. Here, high temperature forming gas anneal means forming gas anneal performed at 600 ^oC which is much higher than the conventional forming gas anneal temperature (~450 ^oC). The HTFG was performed before metal deposition to avoid Al melting and inspire diffusion of forming gas.

Figure 6.10 shows I_d-V_g curves of the MOSFETs for with and without high temperature FG anneal. Subthreshold swing (S) of the MOSFETs with and without the high temperature FG anneal showed 80 and 71 mV/dec, respectively. The reduction of S by the FG gas anneal can be explained by decrease in D_{it} after HTFG [8]. In addition, saturation drain current of the device increased ~ 50% at V_g-V_t = 2.0 V with V_{ds} = 0.5 V after high temperature FG anneal as shown in Fig.6.11.

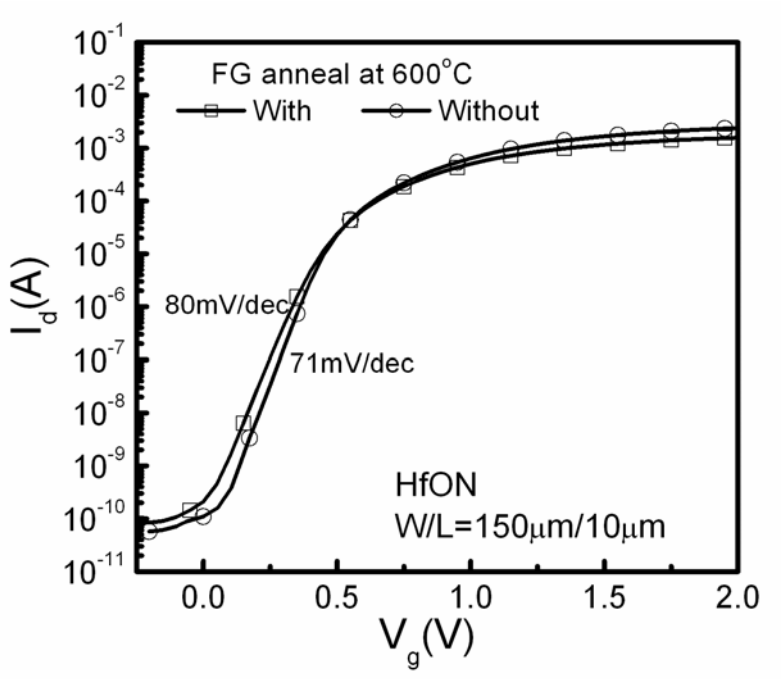

Figure 6.10 I_d-V_g curves of the MOSFETs with HfON gate dielectrics (EOT~13.2Å) for with and without high temperature FG anneal at 600℃ for 30 min.

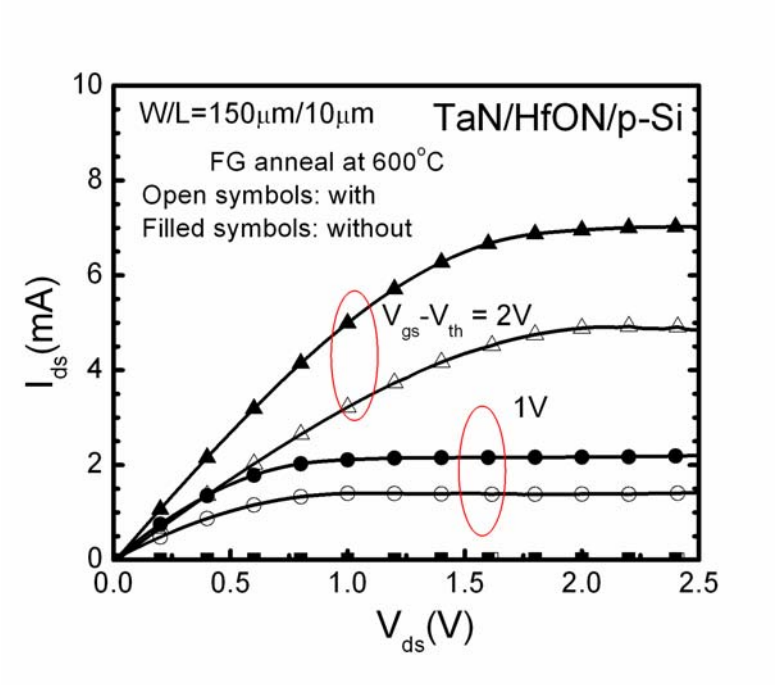

Figure 6.11 I_d-V_g curves of the MOSFETs with HfON gate dielectrics (EOT~13.2Å) for with and without high temperature FG anneal at 600℃ for 30 min.

Figure 6.12 depicts the mobility of HfON nMOSFET with and without FG anneal. HfON shows pretty lower carrier mobility (71 cm^2/Vsec) compared to the values reported for HfO_2 [7]. The reduced mobility of HfON can be attributed to higher fixed charge and interface charge density induced from the incorporated nitrogen, especially low effective field region where Coulombic scattering dominates mobility behavior. By the FG anneal, mobility increased significantly from 71 to 256 cm^2/Vsec at peak. The improvement in the low field mobility by the HTFG can be explained by decrease in D_{it} due to passivation of dangling bonds of HfON. The charge pumping current (I_{cp}) in the inset of Fig.6.12 is proportional to D_{it} by equation [10] (6.4),

$$I_{cp} = 2qD_{it} f \cdot A_G \cdot kT \left[\ln(v_{th} n_i \sqrt{\sigma_n \sigma_p}) + \ln\left(\frac{|V_{fb} - V_t|}{|\Delta V_g|} \sqrt{t_f \cdot t_r} \right) \right], \quad (6.4)$$

where, v_{th} is the thermal velocity of the carrier, n_i is the intrinsic carrier concentration in silicon, σ_n and σ_p are the capture cross sections of electrons and holes, respectively, ΔV_g is the height of the gate pulse, and t_f and t_r are the falling and the rising time of the pulse, respectively. In the measurement of the charge pumping current (I_{cp}), frequency (f) was varied from 10 ~ 100 kHz with fixed other parameters (ΔV_g = 2 V (±1 V), $t_f = t_r$ = 50 nsec, and $A_G = 1.5 \times 10^{-5}$ cm^2).

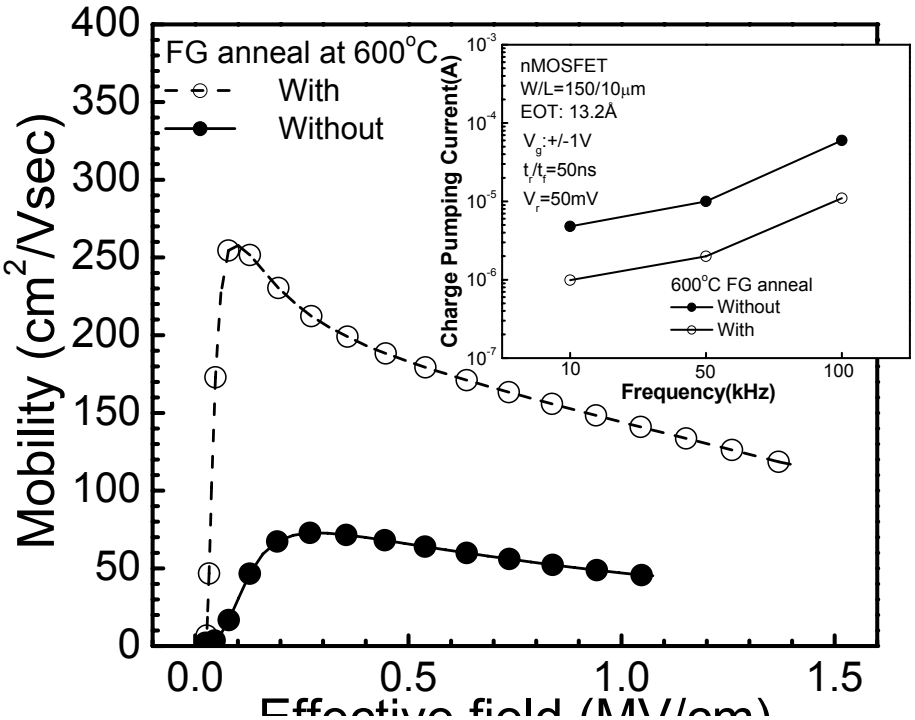

Figure 6.12 Effects of FG anneal at 600°C for 30 min on the mobility and charge pumping current (I_{cp}) of nMOSFET with HfON gate dielectrics (EOT~13.2Å).

6.3 SUPPRESSION OF BORON PENETRATION EFFECTS USING HFON CAPACITORS

The penetration of the boron into the gate dielectric causes a number of problems not only with the quality of the dielectric but especially with the device operation. Boron penetration shifts the threshold voltage of MOS devices to more positive values [11]. During the high-temperature activation annealing, the boron penetrates into and through the gate dielectric. In this experiment, boron penetration was investigated in terms of flat band shift (ΔV_{FB}) of MOS capacitors.

Figure 13 compares B penetration effects in terms of flat-band voltage shifts for HfO_2, BN and HfON films. As a gate electrode, 2000-Å-thick poly-Si was deposited by CVD process using SiH_4 as a precursor and patterned by wet etching process. As a dopant, BF_2 was implanted with a dose of $5x10^{15}/cm^2$ and an energy of 50 keV. Subsequently, annealing by rapid thermal process at 950^oC was performed for varied anneal times. The higher amount of nitrogen, the smaller ΔV_{FB} (i.e. lower boron penetration) was obtained. The result indicates that incorporated nitrogen in the HfON suppresses boron penetrations.

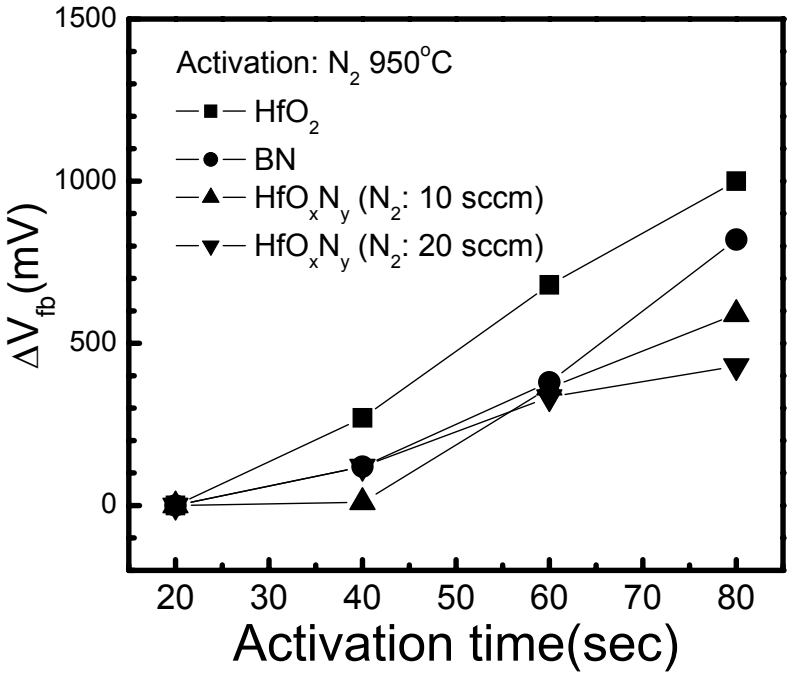

Figure 6.13 Flat band shift (ΔV_{fb}) as a function of dopant activation time at 950°C, N_2 ambient in pMOS capacitor for different dielectrics. ΔV_{fb}'s were compared to flat band voltage of a MOS capacitor annealed for 20 sec for each dielectric.

6.3 SUMMARY AND CONCLUSIONS

Electrical and material characteristics of HfON gate dielectrics were studied in comparison with HfO_2. Incorporated nitrogen in the HfON has been segregated to the dielectric/Si interface. HfON with nitrogen of ~ 5 atomic % at the interface resulted in an increase in crystallization temperature, higher dielectric constant, lower leakage current at the same equivalent oxide thickness (EOT) and high dielectric strength compared to HfO_2. The improved electrical properties of HfON over HfO_2 can be explained by the thicker physical thickness of HfON for the same EOT due to its higher dielectric constant as well as more stable interface layer. Hysteresis of CV curve of HfON capacitor was just slightly higher than that of HfO_2 after PMA anneal. High temperature forming gas anneal at 600^oC for 30 min was effective in improving carrier mobility of nMOSFETs with HfON gate dielectrics. Nitrogen incorporation also turned out to be effective in suppressing boron penetration effects in p^+ poly Si gated MOS capacitors.

6.4 References

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Chapter 7: Effects of nitrogen profiles on MOSFET performances

7.1 MOTIVATION OF NITROGEN PROFILING

Hf-based high dielectric constant (high-k) materials such as HfO_2 [1], their silicates [2, 3], nitrides [4] and silicon-nitrides [5, 6] have been under intense investigation for gate dielectric application into the 70 nm technology nodes and beyond to replace conventional SiO_2 or oxynitrides because of the excessive leakage current and reliability concerns. The Hf-based high-k dielectrics showed compatibility for polycrystalline Si [7], poly-SiGe [8] and TaN gates [9] process in the ultra-thin equivalent oxide thickness (EOT) regimes. However, HfO_2, single oxide high-k dielectrics, has been reported to be vulnerable to the diffusion of oxygen which causes formation of a low-k interfacial layer at the Si interface [9]. In addition, HfO_2 crystallizes at ~600^{o}C, undesirably low for conventional self-aligned source and drain process [10].

Several studies have focused on the improvement of the thermal stability of high-k gate dielectric to overcome the dielectrics' insufficient immunity to oxygen or impurity diffusion during the subsequent thermal process. Those studies include an NH_3 nitridation of Si surface [11], an incorporation of nitrogen into HfO_2 (i.e., hafnium oxynitride: HfON) [4], an addition of Al into HfO_2 (HfAlO) [12], capping a HfO_2 layer with a nitrogen-incorporated layer by plasma nitridation (top nitridation) [13], hafnium silicate (HfSiO) [2, 3] and nitrogen incorporated hafnium silicate (HfSiON) [5, 6].

Among the proposed methods, the incorporation of both Si and N into HfO_2 (i.e. HfSiON, hafnium silicon oxynitride [14, 15]) was found to improve the thermal stability further more effectively than HfON. In the report [10], incorporation of both Si and N into HfO_2 has found to be necessary to increase crystallization temperature and avoid

phase separation at high temperature. However, dielectric constants were reduced in HfSiON due to the presence of silicon oxide bonds with much lower dielectric constant than HfO_2. According to the report of reference [10], HfSiON with optimized composition remained amorphous state up to 1100℃ whereas dielectric constant decreased down to ~10. In terms of application, the HfSiON appears to be very promising materials for the low power devices rather than high speed device requiring further scaling-down of EOTs < 10Å in the near future.

HfON appears to be promising for further scaling-down of EOT since incorporated nitrogen does not degrade dielectric constant of the film. The HfON gate dielectrics turned out to suppress boron diffusion, increase crystallization temperature, and have lower leakage current for the same EOT compared to HfO_2 films [2]. However, nitrogen piles up at the HfON/Si interface which in turns causes mobility degradation as shown in Fig. 7.1. Also, in the bulk of HfON films, only limited nitrogen (~5% at the Si interface) can remain since most of nitrogen in the HfN films during PDA out-diffuses or diffuse into the interface. Therefore, HfON showed insufficient thermal stability for application (i.e. crystallize at ~800^{o}C).

Considering the advantages and disadvantages of incorporating Si into Hf-based dielectrics, it is worth investigating the role of nitrogen and silicon in the dielectrics to optimize EOT, device performance and thermal stability. In this work, nitrogen profile was intentionally modulated in HfON films and the effects of nitrogen profile on the metal-oxide-semiconductor field effect transistor (MOSFET) characteristics were investigated. Interestingly, it also has been known that when Si is incorporated into HfO_2, more nitrogen concentration can be obtained in the film during the deposition and/or PDA process under nitrogen ambient. In this work, silicon layers were inserted into the different positions of HfON films. By doing so, nitrogen profile in HfON films

was modulated and nitrogen amount in the bulk was increased. Electrical characteristics and material analysis of the MOS devices as a function of inserted Si layer will be described in this chapter.

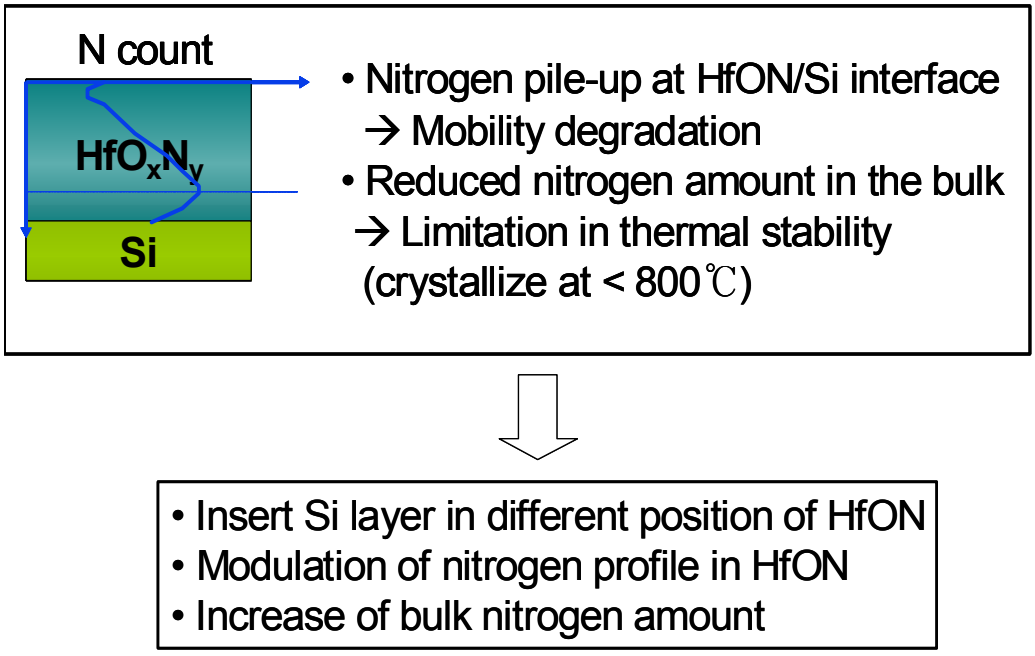

Figure 7.1 Motivation of Si and N incorporation into HfON gate dielectrics

7.2 MODULATION OF NITROGEN PROFILES BY INSERTION OF SI LAYERS

MOS capacitors and MOSFETs of TaN/Hf(Si)ON/p-type Si were used for electrical characterization. Figure 7.2 shows a process flow used for nitrogen profile modulation by inserting a 6Å-thick Si layer into HfON films. As a control sample, HfON was formed on the HF-cleaned Si wafer by a HfN deposition with dc reactive sputtering using a Hf (99.9% purity) target, followed by PDA at 650℃ for 1 min to oxidize the HfN film which was optimized to attain lower EOT with low enough leakage current [3]. To prepare nitrogen profile modulated samples, the first HfN layer was deposited by reactive sputtering in $Ar+N_2$ ambient. Then, a 6Å-thick Si layer was deposited on the HfN layer by sputtering of a pure Si target (6-inch diameter, ~99.999% purity) in Ar ambient. On the Si layer, the second HfN layer was deposited by the reactive sputtering. Immediately after the deposition of the HfN with Si layer, post-deposition-anneal (PDA) was performed using RTA at 650^{o}C, in N2 ambient and for 1 min. In order to investigate the effects of Si and N profile on the electrical properties, the positions of inserted Si layers were changed as shown in Fig. 7.3 keeping the total physical thickness (measured by ellipsometry) approximately 50Å: A) HfON films without a Si layer (control sample), B) bottom, C) middle and D) top position of the HfON in addition to HfON film.

200-nm-thick TaN electrode was used as a gate electrode. Sheet resistance of TaN film was approximately 10 Ω/square. TaN gate was patterned by reactive ion etch (RIE) using a CF_4 as an etching gas. After the gate patterning, phosphorous implantation with an energy of 50 keV and a dose of $5x10^{15}/cm^2$ were performed to form source and drain. Source and drain were activated by annealing at 950℃ for 1 min under nitrogen ambient. Subsequently, deposition of low-temperature oxide (LTO) as

inter-metallic dielectric, formation of metal contact, and Al metallization were done. Before measurement of capacitor characteristics, Al deposition on the back side of the substrate and forming gas anneal at 400℃ for 30 min were performed to ensure lower contact resistance.

C-V curves and leakage current were measured by a HP 4194 LCR meter and a HP 4156B, semiconductor parameter analyzer, respectively. EOT was extracted from the C-V curve measured at 1 MHz after considering the quantum mechanical effect. The area of the capacitor was $5x10^{-5}cm^2$. As material analysis tools, low-energy secondary ion mass spectroscopy (SIMS, model: ATOMIKA 4500), x-ray photoelectron spectroscopy (XPS), and x-ray diffraction (XRD) were used to investigate nitrogen profile, nitrogen amount, and crystallinity of HfON films with and without nitrogen profile modulation, respectively.

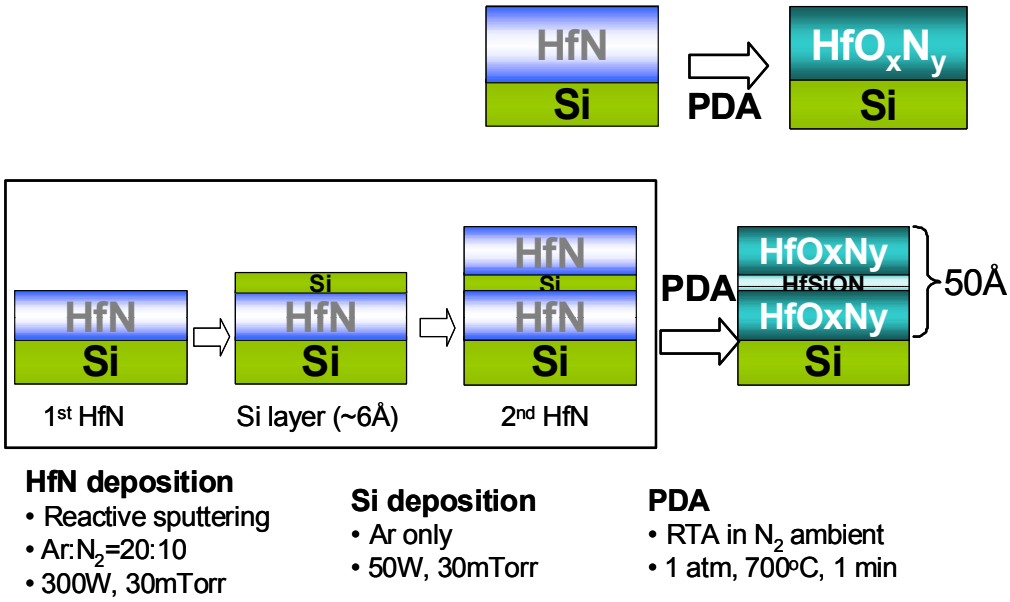

Figure 7.2 Process flow for Si layer insertion into HfN film to modulate nitrogen profile in HfON films.

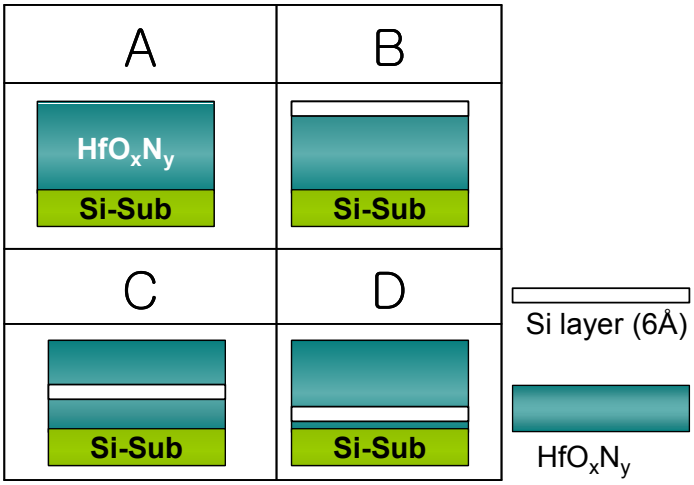

Figure 7.3 Position of Si inserted layers (prior to PDA) used to investigate the effects of silicon and nitrogen profiles on the electrical properties of MOSFET devices. The physical thickness of the four films were maintained approximately 50Å.

7.3 NITROGEN AND SI COMPOSITION PROFILES OF SI INSERTED SAMPLES

Presence of Si is essential to increase nitrogen concentration in Hf-based dielectric films. According to Koyama et al.'s report on HfSiON films prepared by reactive sputtering process under $Ar/N_2/O_2$ ambient, incorporated nitrogen amount can be increased with a higher Si concentration in the film [10]. With Si amounts ([Si]/([Hf]+[Si]) ranging from 60 to 92 atomic %, nitrogen amount was varied from 6 to 30 atomic % in their work. In our work, nitrogen profile in HfON films was modulated by inserting a thin Si layer in the dielectrics. Nitrogen concentration as a function of XPS incident beam angles was depicted for different inserted Si positions in Fig. 7.4. Two observations can be made: a) by inserting a Si layer, nitrogen composition was increased compared to HfON films and b) as Si layer was placed further from the Si interface, the nitrogen concentration of the dielectrics increased. The first observation can be attributed to the presence of Si that traps nitrogen. The second observation indicates that the inserted Si layer makes it difficult for the nitrogen in the HfN films to diffuse out from the bulk.

Low energy secondary ion mass spectroscopy (SIMS) was used to investigate Si and N profiles. Figure 7.5 shows low energy SIMS depth profiles of Si and SiN which reflect Si and N profiles in the dielectric films of the control (HfON) and samples with Si layers near the top and bottom interfaces as schematics in the inset. As primary ion species, Cs^+ ions with an energy of 400 eV and incident ion beam angle of 40 degrees were used. As expected from the angle-resolved XPS analysis, Si and N counts were enhanced in the Si-inserted HfON films compared to the HfON films. SIMS profiles of Si and SiN in Fig. 7.5 correspond well with the positions of the inserted Si layers. The

SIMS profiles indicate that the method used in this study modified nitrogen profiles controllably.

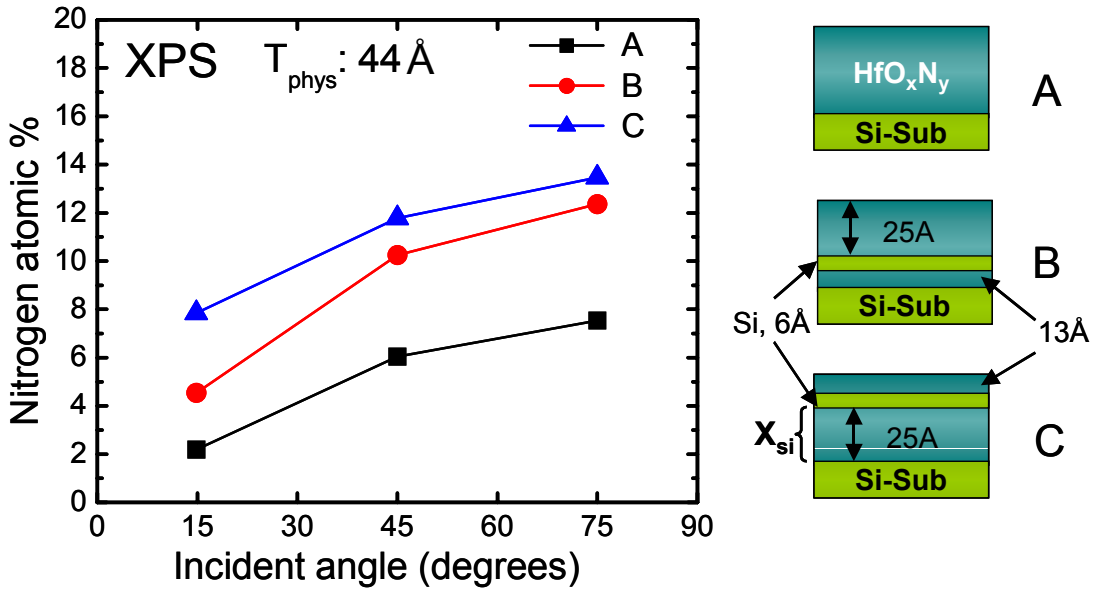

Figure 7.4 Nitrogen concentrations in HfON films as a function of XPS incident beam angles for different inserted Si positions.

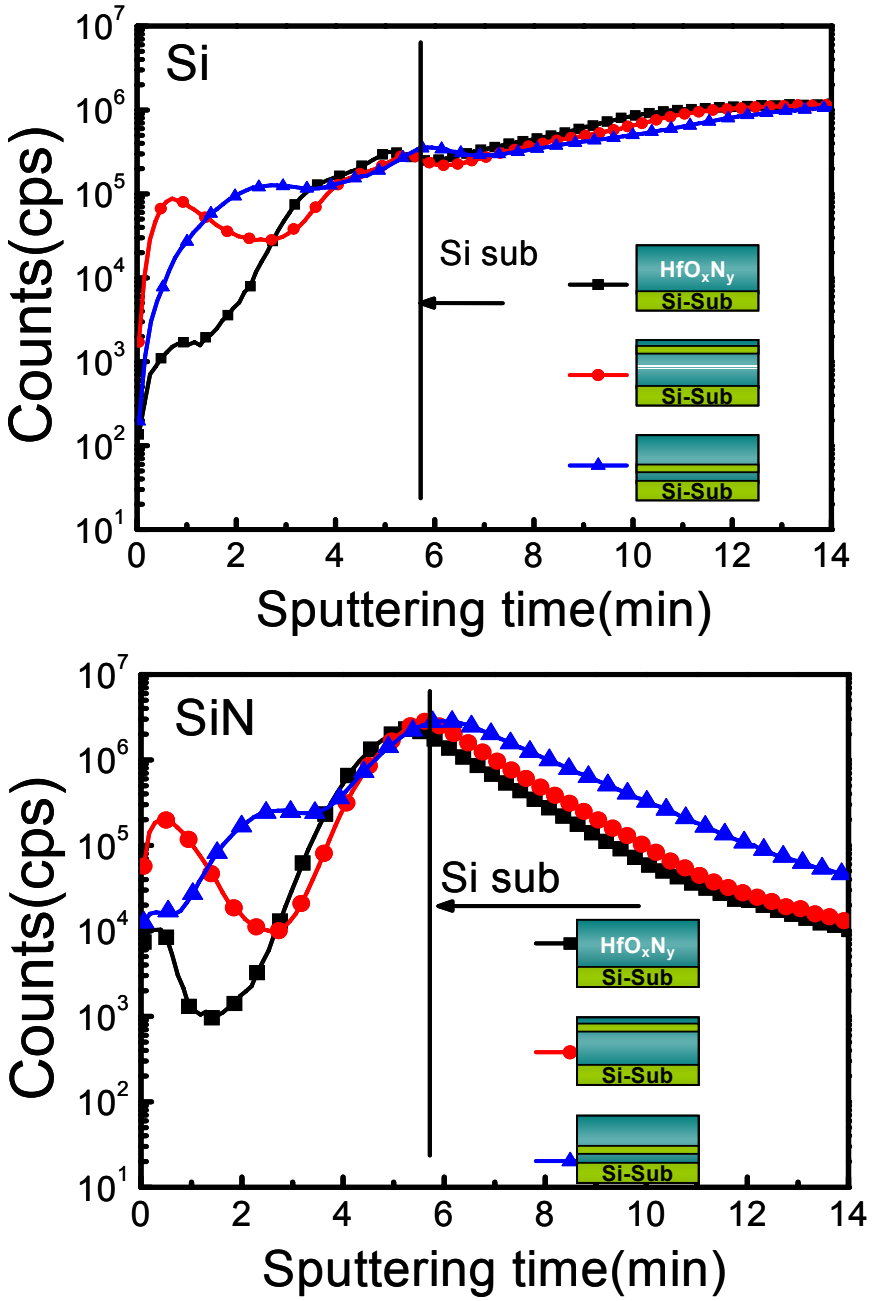

Figure 7.5 Low energy SIMS profiles of Si (upper) and SiN for the HfON films on the Si substrates with different Si inserted layers. Nitrogen was detected using SiN peaks.

7.4 EFFECTS OF SI INSERTION ON CRYSTALLIZATION TEMPERATURE

XRD peaks of 108Å-thick HfON film and 112Å-thick Si inserted sample were investigated as a function of PDA temperature ranging from 500°C to 1000°C. Substrates are (100) Si wafers. In Fig. 7.6, HfON showed crystallized peaks above ~ 700 °C. In particular, XRD peaks of HfON films became sharper and more evident by an anneal at 1000 °C. Compared to the HfON, Si-inserted HfON shows very slight XRD peaks for a temperature of 1000 °C. The XRD peaks of Si inserted HfON annealed at the 1000 °C were smaller than those of the HfON films. Koyama et al. reported that HfSiON with higher concentration of Si and nitrogen ([Si] = 74 ~ 80 at. % and [N] = ~ 30 at. %) remained amorphous even after PDA at 1000 °C [10]. Lower concentration of silicon (~10 at. %) and nitrogen (< 8 at. %) in this work can be attributed to the slightly lower crystallization temperature of Si inserted-HfON.

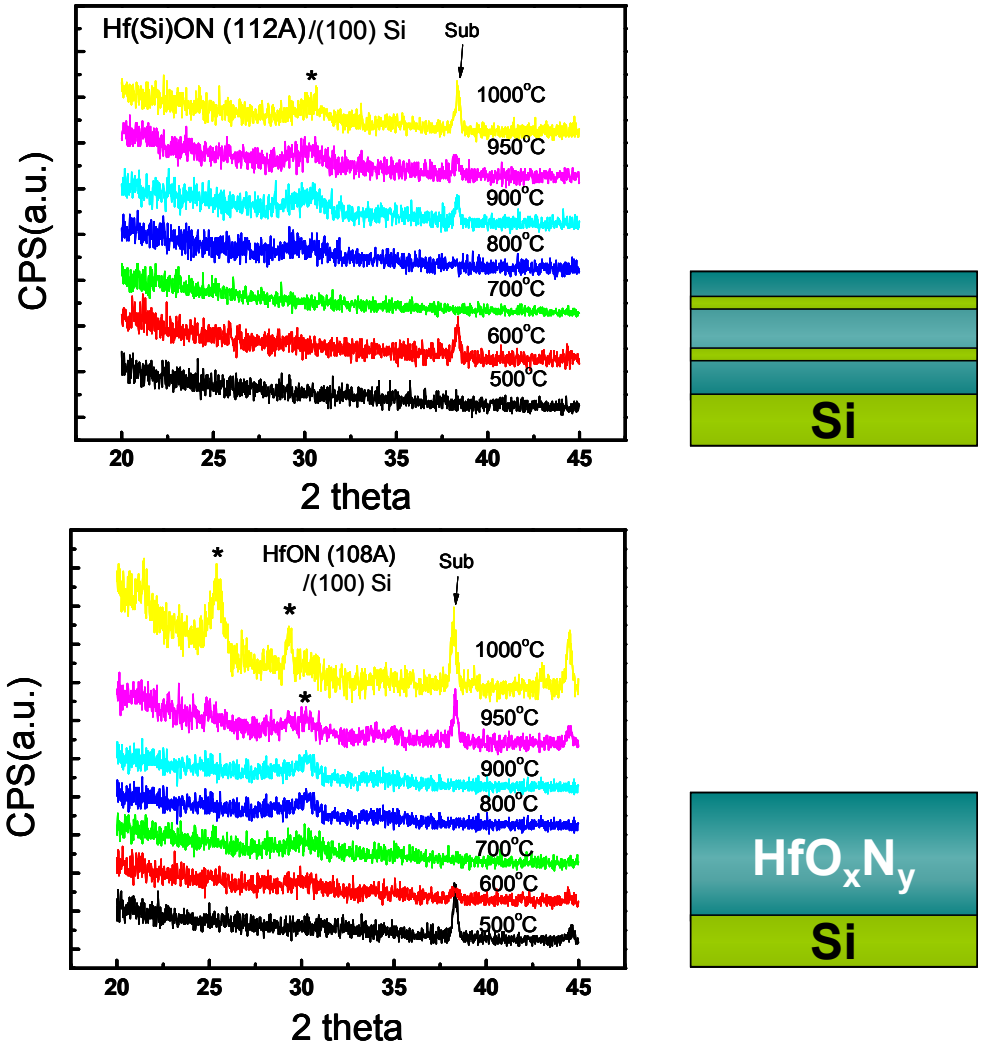

Figure 7.6 Comparison of XRD peaks between the control (HfON) and Si-inserted HfON films deposited (100) Si substrates. X-ray measurement was performed using thin film mode (α=3°, Cu K α, 30mA, 30kV).

7.5 EFFECTS OF NITROGEN PROFILE MODIFICATION ON THE ELECTRICAL PROPERTIES OF HF-BASED DIELECTRICS

Figure 7.7 describes the leakage current density measured at –1.5V as a function of EOTs for different Si-inserted nMOS capacitors in addition to those for HfO_2 and HfON. Among the four samples, sample B showed the thinnest EOT while the other three samples (A, C, D) showed similar leakage current for the same EOTs. The thinnest EOT was obtained at the HfON with inserted Si layer on the top. This can be attributed to the highest nitrogen concentration as shown in Fig. 7.5. The more nitrogen incorporation results in the higher dielectric constant in HfSiON gate dielectrics.

Figure 7.8 (a) compares EOT increase due to PMA at 900^{o}C, 1 min under N_2 ambient and Fig. 7.8 (b) shows leakage current density and EOT as a function of dielectric types. As expected, EOT increased due to the PMA anneal. Compared to the control sample (HfON), Si inserted sample showed reduced EOT changes (<0.5Å). The reduction of EOT increase in the Si inserted samples indicates that increased amount of nitrogen and silicon led to the suppression of oxygen diffusion which may cause the formation of the low-k layer at the dielectric/Si substrate interface. Difference in leakage current density is negligible between dielectric groups. The results indicate that the higher nitrogen concentration in the Si inserted samples are more effective in obtaining thinner EOTs while remaining the same order of leakage current density.

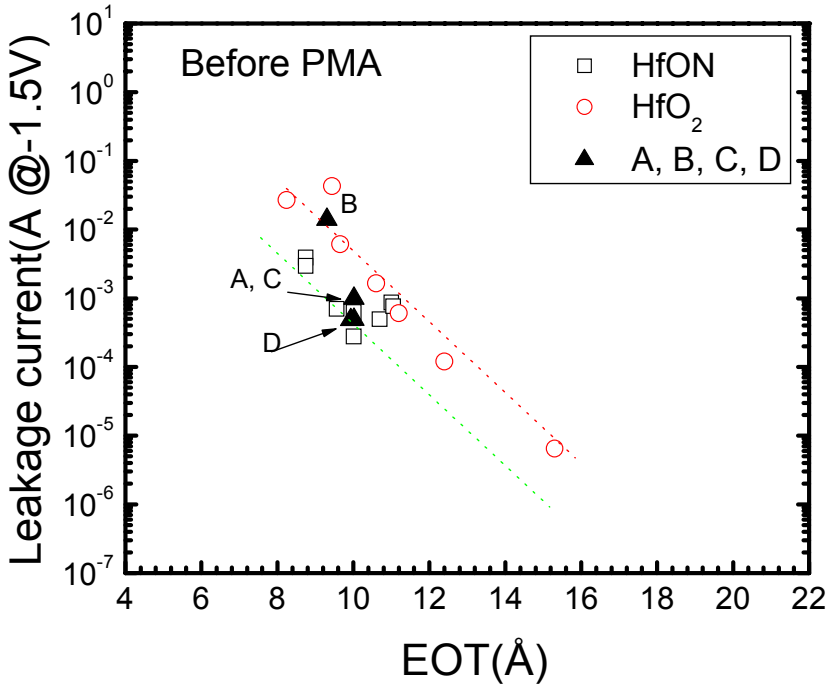

Figure 7.7 Leakage current density measured at V_g=–1.5V as a function of EOTs for different Si-inserted nMOS capacitors.

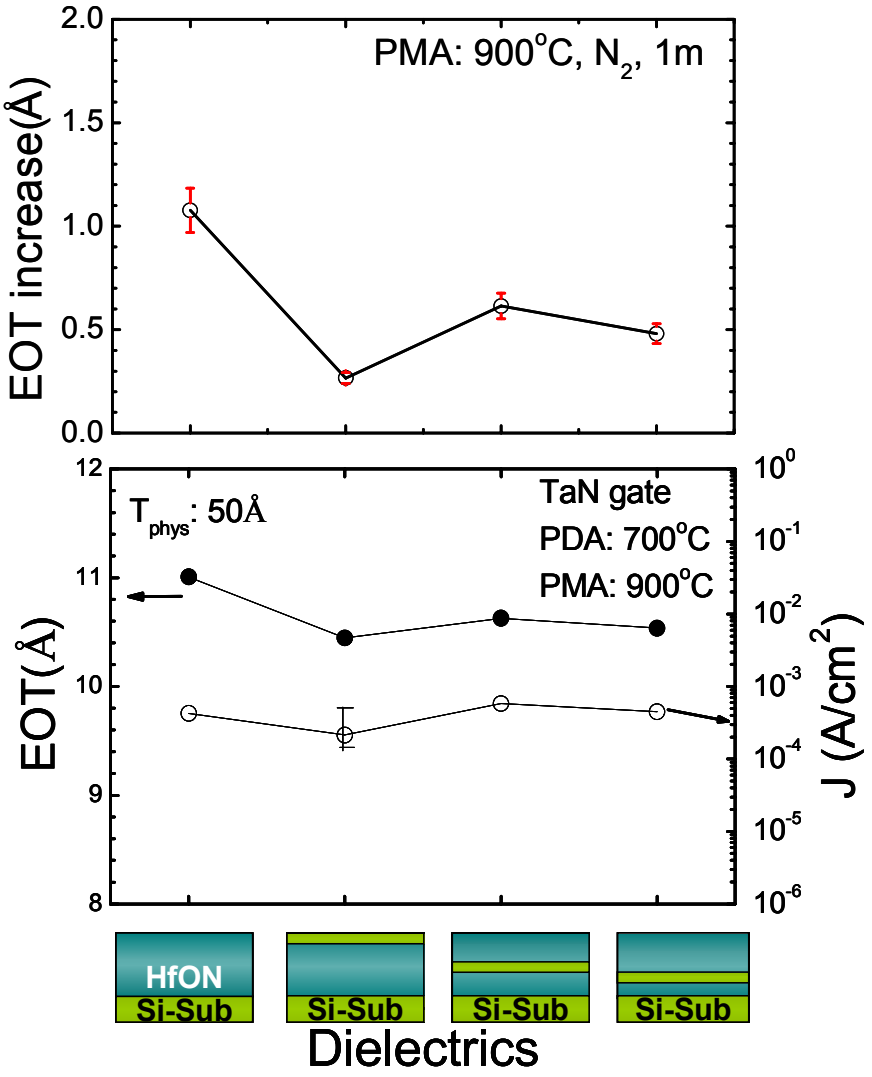

Figure 7.8 (a) EOT increase after PMA anneal at 900°C, 1 min under N_2 ambient. Compared to the control sample (HfON), Si inserted sample shows reduced EOT increase. (b) EOT and leakage current density for different dielectrics. Si inserted ones show reduced EOTs with a small difference (<0.5Å). Difference in leakage current density is negligible between dielectric groups.

7.5 HYSTERESIS

Hysteresis of MOS capacitor indicates the difference in the CV curves measured with a gate voltage swing from inversion region to accumulation region and vice verse. In the case of Hf-based dielectrics, the CV curve of the upward gate voltage swing (i.e. from negative voltage to positive voltage, that is, from accumulation region to inversion region) is shifted to the negative side compared to the downward voltage swing. Quantitatively, hysteresis is represented by a difference in the flat band voltage (ΔV_{fb}) of two CV curves measured by downward and upward voltage swing at a given voltage span. The origin of the hysteresis is believed to be charge trapping and de-trapping in the dielectric film [5]. Therefore, hysteresis measurement is a useful tool to obtain information on the quality of dielectric film.

Figure 7.9 shows hysteresis of CV curves for the capacitors with the varied Si positions before and after PMA at 900^{o}C, 1 min, under N_2 ambient. Hysteresis was measured after three times of voltage sweep from 1V to -2.0V at 1MHz of ac voltages. In the case of without-PMA, there is a clear trend among the Si inserted capacitors: as the Si layer is placed the closer to the Si substrate interfaces, the higher hysteresis was obtained. This result indicates that the nitrogen-incorporated layer by the Si incorporation is responsible for the hysteresis trends explained by equation (7-1) [18],

$$\Delta V = -(d - x_{ot})\frac{Q_{ot}}{\varepsilon_i} \quad (7\text{-}1),$$

where d, x_{ot}, and Q_{ot} represent dielectric thickness, distance of the trap layer from the substrate assuming the trap layer as a very thin sheet, and trap charge density,

respectively. Nitrogen incorporated layer which has been known to induce trap sites has more effects on flat band changes as the layer becomes the closer to the Si substrates. Also, it is worth noting that "sample B" which has higher nitrogen concentration than HfON shows little difference in the hysteresis compared to the control sample. The results suggest that Si compensates trapping enhanced by nitrogen incorporation in the Hf-based dielectrics.

After PMA, hysteresis was reduced significantly for all the samples. In this case, HfON has the smallest hysteresis due to the highest EOT increase after PMA, indicating the formation of the thickest low-k interfacial layer among the samples. The difference between Si inserted samples was negligible probably due to the intermixing of the Si layer during the PMA anneal.

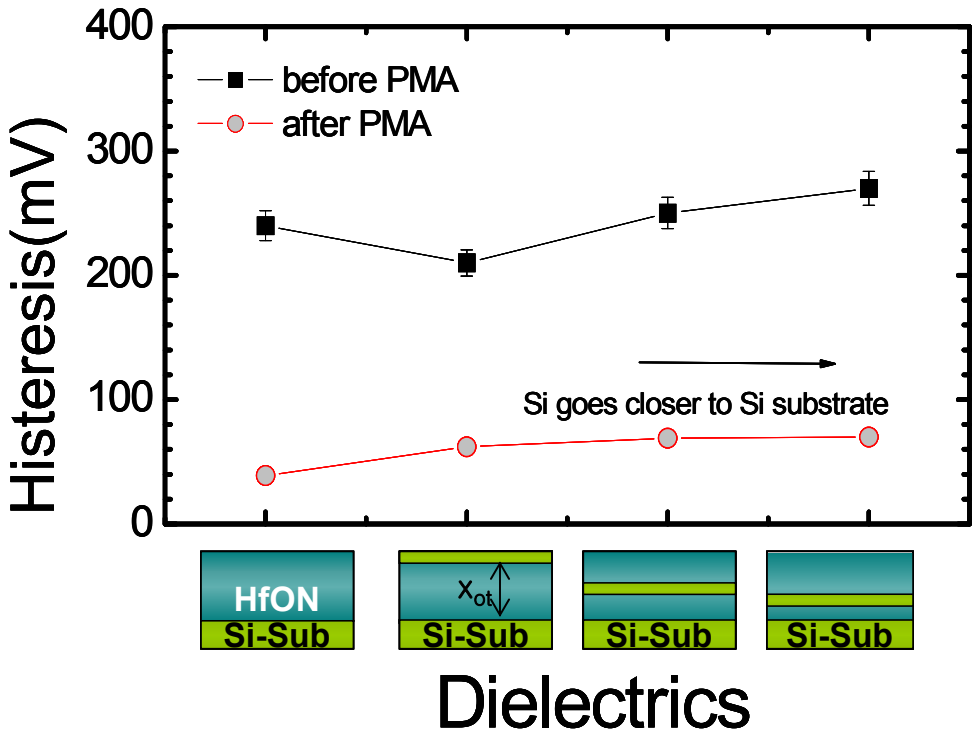

Figure 7.9 Hystersis before and after PMA at 900°C, 1 min, under N_2 ambient. Hysteresis was measured after three times of voltage sweep from 1V to -2.0V at 1MHz of ac voltages.

7.5 TRANSISTOR PERFORMANCE

Transistor performance was compared using TaN-gated nMOSFETs with 10μm/150μm of gate length/width. Figure 7.10 shows I_d-V_d characteristics measured at V_g-V_t=2.0V for different dielectrics. Threshold voltage (V_t) of the MOSFETs with the four different dielectrics were ~0.3V with a small difference (less than <10mV) in V_{th} among different groups. As shown in Fig. 7.10, Si inserted dielectrics showed improved saturation drain current (Id_{sat}) compared to the HfON. In particular, Id_{sat} of "sample C" is ~55% improved compared to the HfON although EOTs of the two MOSFETs are very similar. "Sample C" was the sample in which Si layer was placed in the middle of HfON film : it showed the highest Id_{sat} normalized for EOT as shown in the inset of Fig. 7.10. The results indicate that excessive nitrogen concentration or having nitrogen layer placed too closer to the Si interface is undesirable in terms of MOSFET performance. Also, addition of Si in the HfON film contributes to the compensation of the adverse effects of nitrogen in the MOSFET performance.

Figure 7.11 depicts the mobility of nMOSFET with different dielectric groups as a function of effective gate voltage. As expected from the trend in I_d, Si inserted samples show improved carrier mobility compared to HfON for both low and high effective field range. Sample C showed the highest channel carrier mobility.

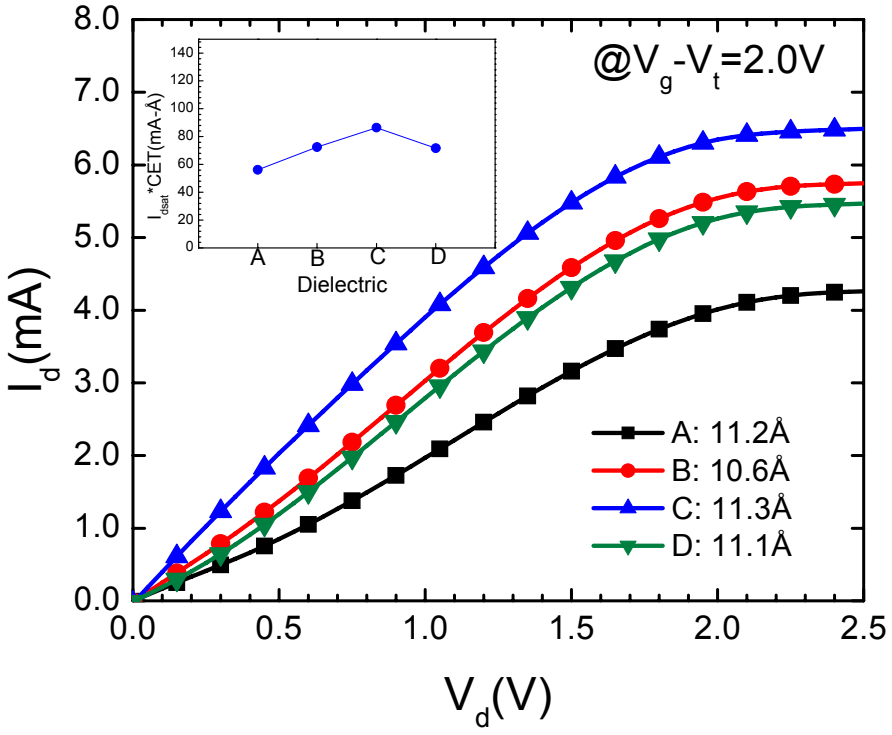

Figure 7.10 Drain current (Id) as a function of drain voltage (Vd) of nMOSFET devices with different dielectric. HfON gate dielectrics with Si inserted layers show improvement in saturated drain current (Id_{sat}) as well as saturated drain current normalized to CET.

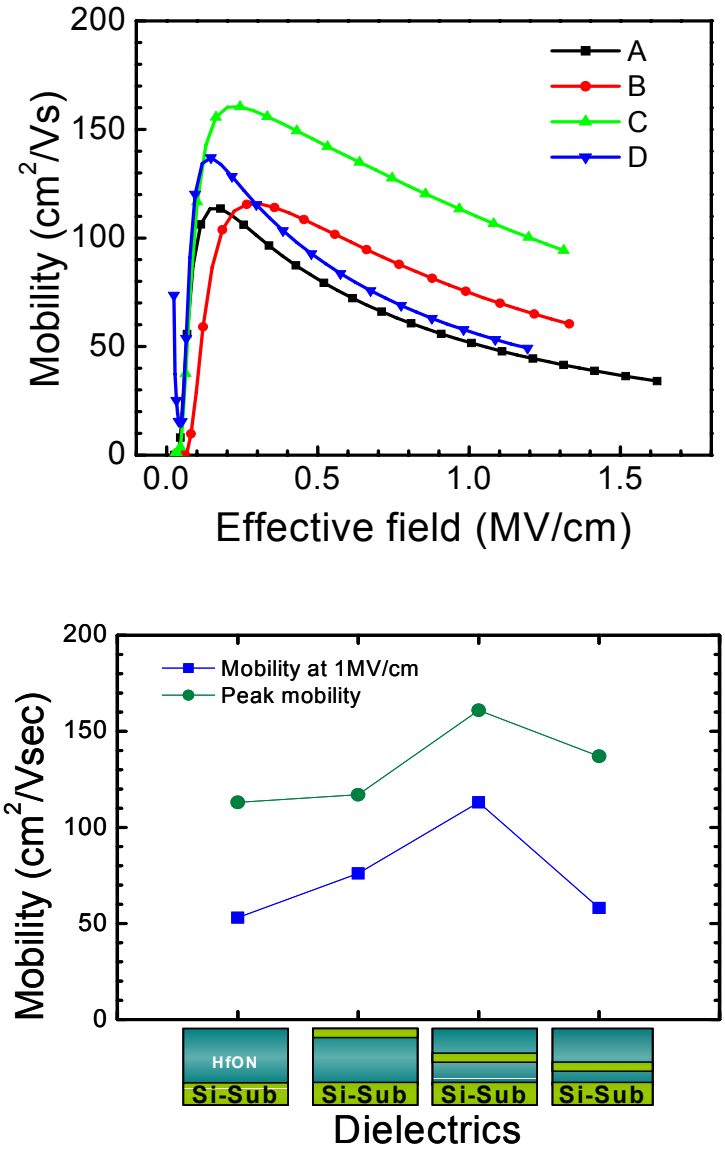

Figure 7.11 Mobility as a function of effective vertical field (E_{eff}) for nMOSFETs with different dielectric groups (upper) and peak mobility and high field mobility @E_{eff}=1.0MV/cm (down).

7.6 SUMMARY

The effects of silicon and nitrogen profiles in gate dielectrics on the electrical and material properties of the Hf-based dielectric were investigated. To vary nitrogen profiles in the HfON films, 6-Å-thin Si layers were placed on the different position of HfON films. By the insertion of Si layer, nitrogen profiles were modulated. The inserted Si resulted in increased thermal stability. As the position of Si layer becomes further from the Si substrates, hysteresis decreased. Highest mobility was observed at the dielectrics with Si layer inserted in the middle of HfON films.

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Chapter 8: Conclusions and Future Works

8.1 SUMMARY AND CONCLUSIONS

In this dissertation, most efforts were devoted to the investigation of nitrogen incorporated hafnium-based high-k dielectrics compared to HfO_2 oxide for the application into the future gate dielectric materials. In addition, TaN, a promising metal gate for the high-k dielectrics, and effects of Hf into the conventional Si process were described. Compared to HfO_2, nitrogen incorporated hafnium oxide showed improved thermal stability and superior scalability in terms of leakage current vs. EOT.

HfO_2 have been under intense investigation for gate dielectric application into the 70 nm technology nodes and beyond to replace conventional SiO_2 or oxynitrides since it possesses a dielectric constant of 22 – 25, a large band gap of 5.6 eV with sufficient band offsets of larger than 1.5 eV, and is thermally stabile in contact with silicon and metal gates. However, HfO_2 is vulnerable to the diffusion of oxygen that causes formation of a low-k interfacial (silicon oxide or silicate) layer at the Si interface and boron penetration when combined with the p^+ poly-Si gate technology. EOT of HfO_2 with an initial EOT of ~10 Å increase more than ~4Å during the post-metal-deposition anneal (PMA) at ~950 ºC. This EOT increase would limit the use of high-k dielectrics. In addition, HfO_2 crystallizes at relatively low temperature (<600 ºC) unlike SiO_2 that remains in amorphous phase through the semiconductor process.

The effects of Hf implanted into p-type Si substrates on the properties of n^+ polycrystalline-Si/SiO_2/Si capacitors and MOSFETs have been investigated. Flat-band voltages (V_{fb}) and substrate doping concentrations (N_A) calculated from high frequency C-V curves of the capacitors was not dependent on the doses of Hf. Also, electron channel mobility was not degraded by Hf contamination. The amount of Hf diffused

into Si substrate during the high-k dielectric imposed negligible effects on silicon based MOS device characteristics.

In this work, sputtered-TaN was mainly used as a gate electrode. Work functions of TaN Tantalum nitride (TaN) film before and after post-metal-annealing were ~ 4.15eV, and ~ 4.7 eV, respectively.

Surface nitridation technique using NH_3 anneal has been investigated to reduce interface reaction and consequently the equivalent oxide thickness (EOT) of TaN/HfO_2/ Si MOS capacitor. For the same EOT, the nitrided samples showed 1 ~ 2 order of magnitude lower leakage current density compared to the non-nitrided ones. Furthermore, the nitrided samples showed better thermal stability. However, nitridation induced higher interface state density and larger hysteresis. The degraded interface quality due to the nitridation was improved by post-metal annealing (PMA). Using the optimized nitridation and PMA, EOT of the capacitor was scaled down to ~10 Å with keeping leakage current below 0.1 mA/cm^2 at –1.5V. Interface state density (D_{it}) and hysteresis (ΔV) were ~8.4x10^{10} eV^{-1}/cm^2, and 45 mV, respectively.

Electrical and material characteristics of hafnium oxynitride (HfON) gate dielectrics have been studied in comparison with HfO_2. HfON was prepared by a deposition of HfN followed by post-deposition-anneal (PDA). By secondary ion mass spectroscopy (SIMS), incorporated nitrogen in the HfON was found to pile up at the dielectric/Si interface layer. Based on the SIMS profile, the interfacial layer (IL) composition of the HfON films appeared to be similar to hafnium-silicon-oxynitride (HfSiON) while the IL of the HfO_2 films seemed to be hafnium-silicate (HfSiO). HfON showed an increase of 300℃ in crystallization temperature compared to HfO_2.

HfON with nitrogen of ~ 5 atomic % at the interface resulted in an increase in crystallization temperature, higher dielectric constant, lower leakage current at the same

equivalent oxide thickness (EOT) and high dielectric strength compared to HfO_2. The improved electrical properties of HfON over HfO_2 can be explained by the thicker physical thickness of HfON for the same EOT due to its higher dielectric constant as well as more stable interface layer. Hysteresis of CV curve of HfON capacitor was just slightly higher than that of HfO_2 after PMA anneal. High temperature forming gas anneal at 600^{o}C for 30 min was effective in improving carrier mobility of nMOSFETs with HfON gate dielectrics.

The effects of silicon and nitrogen profiles in gate dielectrics on the electrical and material properties of the Hf-based dielectric were investigated. To vary nitrogen profiles in the HfON films, 6-Å-thin Si layers were placed on the different position of HfON films. By the insertion of Si layer, nitrogen profiles were modulated. The inserted Si leading to the nitrogen incorporation increased thermal stability. As the position of Si layer becomes further from the Si substrates, hysteresis decreased. Highest mobility was observed at the dielectrics with Si layer inserted in the middle of HfON films.

8.2 SUGGESTION FOR FUTURE WORKS

The works in this dissertation has been focused on the process development of nitrogen incorporated HfO_2 and confirmation of their advantages in terms of thermal stability, scalability and performance of MOS capacitor/transistors for gate dielectric application into the 70 nm technology nodes and beyond. Future work can be categorized as follows to continue and improve the related fields.

❖ Further Scaling

Since HfON shows ~ 100 times smaller J compared to HfO_2 as described in chapter 6, HfON has higher possibility for the further scaling down of EOT. However, preliminary results showed that scaling down of physical thickness without optimizing PDA condition does not lead to the reduction of EOT. Figure 8.1 plots physical thickness of HfON films after PDA vs. as-deposited thickness. Physical thickness of HfON thicker than ~ 44 Å increases by ~2.5 Å after PDA, while the increase of HfON thinner than ~44 Å is enhanced as the film becomes thinner. This means that for a thinner HfON film, the thermal budget of the PDA condition (650 ºC, N_2, 1 min) is large enough to induce EOT increase due to the penetration of oxygen through the HfON film.

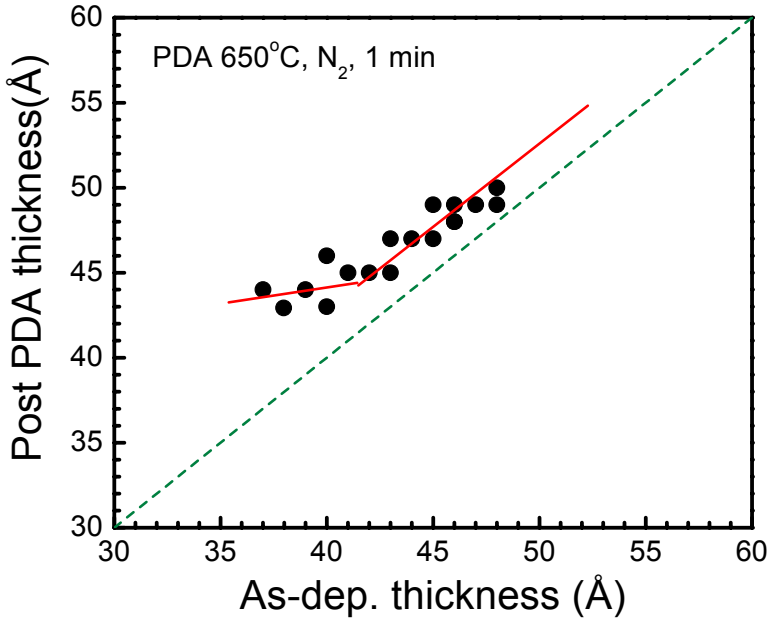

Figure 8.1. Physical thickness change after PDA anneal for a various initial thickness of HfON.

PDA thermal budget which were too high for the thin HfON time was reduced. Fig. 8.2 and Fig. 8.3 show C-V curves and J-V curves for different PDA times at 650 ºC for 1 min under N_2 ambient, respectively. Shorter PDA time provides reduced EOT without a serious sacrifice of increased leakage current. Further research is required to scale down EOT of HfON films from the respective of PDA annealing process.

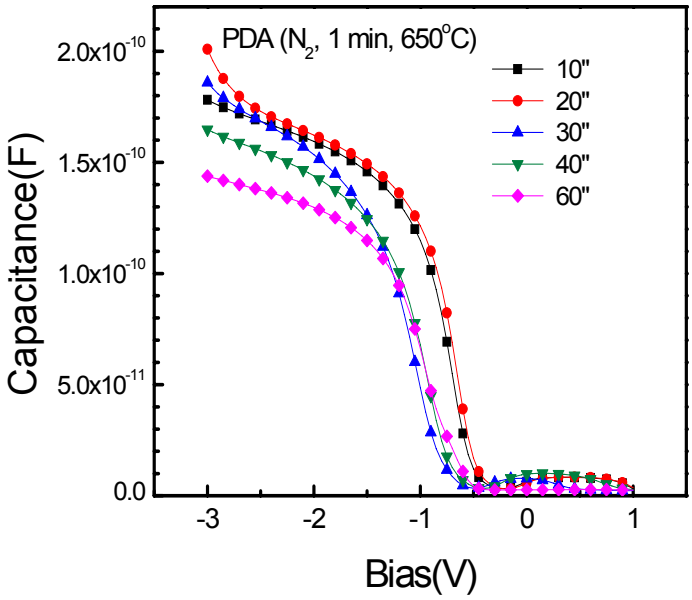

Figure 8.2 C-V curves of HfON dielectrics with varied PDA time.

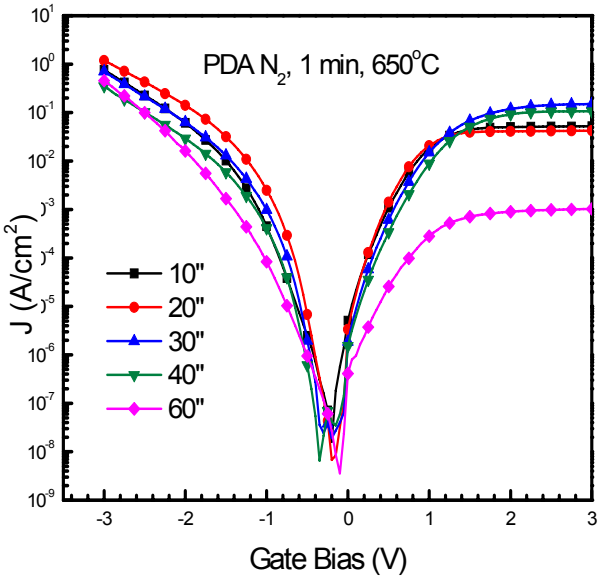

Figure 8.3 J-V curves of HfON dielectrics with varied PDA time.

❖ Improvement of HfON/Si interface

The clear goal of interface engineering in the high-k gate stack is to achieve a sufficiently high-quality interface with the Si channel, as close as possible to that of SiO_2. The state-of-the art SiO_2 has very low interface state density (~$2x10^{10}$ $eV^{-1}cm^{-2}$). D_{it} values of all the films investigated (i.e. HfO_2, HfON, HfO_2 capped with nitrogen incorporated layer, and NH_3 surface nitrided HfO_2) were in the range of 6–$8x10^{10}eV^{-1}cm^{-2}$ as shown in Fig. 8.4.

Shift of flat band voltage (V_{fb}) is undesirable and must be minimized to attain reproducible and stable transistor operation. For the same reason, hysteresis of C-V is required to be less than 20 mV to suppress V_{th} instability. High hysteresis of HfON without PMA (~300 mV) was reduced considerably down to ~50mV after PMA. The origin of hysteresis may be attributed to fixed charge, bulk trapped charge and interface traps, but there has not been clear explanation reported so far. Further research on the origin of the hysteresis and surface states is required. In addition, further optimization of the dielectric process and annealing condition will be pursued to reduce D_{it} and hysteresis of the HfON films.

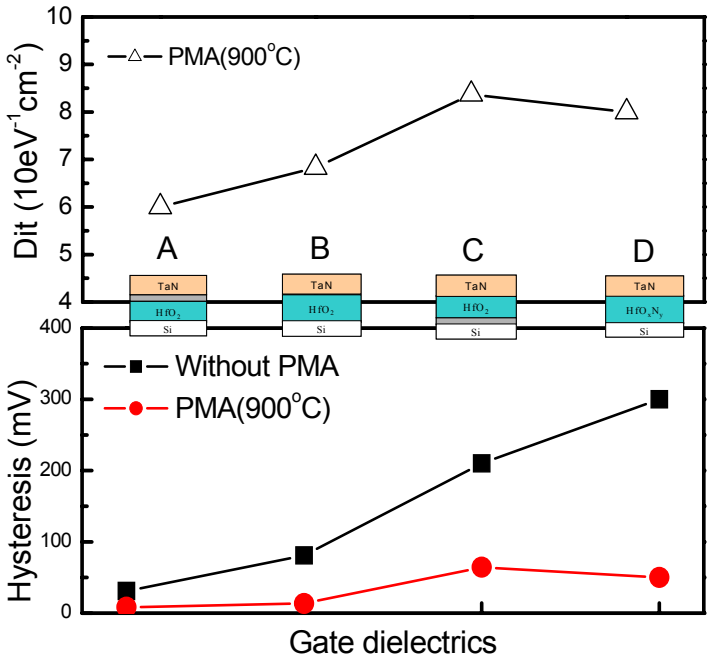

Figure 8.4. Hysteresis variations as a function of dielectrics (A: HfO_2 capped with nitrogen-incorporated layer, B: HfO_2 C: HfO2 with surface nitridation, D: HfON).

❖ Gate electrodes with HfON devices

In this dissertation, TaN gate was mostly used as a gate electrode. Compatibility of nitrogen incorporated dielectrics with other possible electrodes for high-k application such as poly-Si, TaSiN, Ru, and other metal electrodes needs to be investigated.

❖ Reliability of HfON devices

Comprehensive studies on the reliability of nitrogen incorporated dielectrics are essential for their application. The studies may include 1) time dependent dielectric breakdown (TDDB) using dc, uni-polar, and polar stress, 2) stress induced leakage current (SILC) 3) degradation of transistor characteristics by voltage stress such as negative/positive bias temperature instability (NBTI/PBTI) and hot carrier stress, and etc. for different nitrogen positions and/or contents.

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Vita

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